ELECTROSTATIC DISCHARGE CONSIDERATIONS

GENERAL

The purpose of this document is to provide information relative to considerations of Electrostatic Discharge (ESD) during the testing, inspection, manufacturing, assembling, packaging and general handling of electrical or electronic parts, assemblies, and equipment. As a general rule, the guidelines and requirements specified in MIL-STD-1686, "Electrostatic Discharge Control Program for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)" and MIL-HDBK-263, "Electrostatic Discharge Control Handbook for Protection of Electrical and Electronic Parts, Assemblies and Equipment (Excluding Electrically Initiated Explosive Devices)" provide excellent guidelines in ESD management and protection of electronic parts. MIL-STD-1686 covers the establishment and implementation of an ESD Control Program and MIL-HDBK-263 provides guidance for the establishment and implementation of an ESD Control Program in accordance with MIL-STD-1686.

Electrostatic Discharge may be defined as the transfer of electrostatic charge between bodies at different potentials, caused either by direct contact, arcing or induction. Electrostatic charges can be generated by the simple everyday activities e.g. relative motions, physical separation of materials or flow of solids, liquids, or gases. Materials which are prime generators of electrostatic voltages include, but are not limited to, common plastics such as polyethylene, vinyl, foam, polyurethane, synthetic textiles, fiberglass, glass, rubber, and many more commonly used materials. Damaging electrostatic voltages are commonly generated by contact and subsequent separation of these materials by industrial processes and the movement of involved personnel.

Much of industry and many users of electronic components are familiar with the damage that static electricity can impose on metal oxide semiconductor (MOS) devices. However, the susceptibility of other part types and semiconductor technologies to ESD damage has been demonstrated through use, testing, and failure analysis. As technologies are developed and the use of new materials increases and the densities of devices decrease, increased susceptibility to ESD is likely. A number of ESD-sensitive (ESDS) electrical and electronic parts have been identified, including microelectronic, discrete, and integrated semiconductor devices; thick and thin film resistors, chips and hybrid devices; and piezoelectric crystals. In addition, electronic assemblies, subassemblies, and equipment containing these types of parts are also considered to be ESDS.

Recommend the above referenced documents be used to further investigate specific issues and concerns relative to the effects of ESD on electrical and electronic parts. The focus of this document will be to discuss ESD considerations specific to the technologies identified and discussed in this manual.

ESD FAILURE TYPES

Parts that are susceptible to ESD failures include any logic family in which only small energies are required to switch states, or small changes of voltage in high impedance lines are experienced. Examples of technologies which are ESDS include N-channel MOS (NMOS), P-channel MOS (PMOS), Complementary MOS (CMOS), and low power Transistor-Transistor Logic (TTL). Other technologies, which may be ESDS, include linear circuits with high impedance and high gain inputs, Radio Frequency (RF) amplifiers, and other RF components at the equipment level. Protecting ESDS parts at the equipment level requires good RFI/EMC design, bus buffering, proper termination of buses, shielding of bus conductors and the avoidance of penetrations of the equipment cabinet that lead to sensitive parts. ESD can cause intermittent, transient, catastrophic, or latent defects, which can eventually become a catastrophic failure.

Intermittent Failures

Intermittent failures, also known as upset failures, can occur on certain part types such as Large Scale Integration (LSI) memories. Such failures occur when equipment is in operation and is usually characterized by a loss of information or temporary distortion of its functions. No apparent hardware damage occurs and proper operation resumes after the ESD exposure. In the case of some digital equipment, proper operation resumes only after re-entry of the information by re-sequencing the equipment.

Transient Failures

Transient failures, or hard failures as they are sometimes known, can be the result of the electrical noise associated with an ESD spark in the vicinity of the equipment. The electrical noise may enter the equipment by either conduction or radiation. Equipment operation is upset if the ESD-induced voltage and/or currents exceed the signal levels in the electronic circuit. In high impedance circuits the signals are voltage levels, thus capacitive coupling will dominate and ESD-induced voltage will be the major problem. In low impedance circuits, the signals are current-based, thus inductive coupling will dominate and the ESD-induced currents will be the major problem. Since the voltages and currents required to cause damage are one to two orders of magnitude greater than those required to cause upset, damage is more likely when there is conductive coupling. Radiated coupling will normally cause upset failures only.

Catastrophic Failures

Transient failures occur while equipment or parts are in operation. Catastrophic failures, on the other hand, can occur at any time. Catastrophic ESD failures, also

known as hard failures, can be caused by a number of electrical overstress conditions such as discharge from a person or object that comes into contact with the equipment or part, the presence of an electrostatic field, or a high voltage spark discharge. Occasionally, some catastrophic failures may not occur until after multiple ESD events.

Latent Defects

Unfortunately many parts are marginally damaged by ESD events, and the hard failures do not occur until operating stress over time causes further degradation. This is the defect of greatest concern since it cannot be detected or screened.

PRODUCT FROM TECHNOLOGIES AFFECTED BY ESD DAMAGE

Products from different technologies are susceptible to ESD damage in varying degrees. The following describes the effects of ESD damage on different products:

Metal-Oxide Semiconductor Structures

Integrated circuit MOS technologies that are susceptible to ESD damage include NMOS, CMOS, and PMOS structures, as well as variations of these structures such as metal-gate, silicon-gate, and silicon on sapphire (SOS). Certain bipolar linear integrated circuit operational amplifiers employ MOS capacitors on their monolithic chip and these capacitors are susceptible to dielectric breakdown caused by ESD. Operational amplifiers whose capacitors do not have apparent direct contact to external pins are less vulnerable than parts whose capacitors are placed directly across an external pin combination. Hybrid microcircuits can employ a chip capacitor which is a MOS structure containing a dielectric, which is vulnerable to ESD. MOS chip capacitors should not be used in hybrid devices since other chip capacitors are available, which are not considered as ESDS devices.

ESD occurrences can damage the oxide in MOS structures because their breakdown voltage is low compared to voltage levels experienced with ESD. Breakdown of the oxide insulator results in catastrophic damage as opposed to breakdown of a semiconductor, which may be reversible. As the dielectric punch-through occurs, the metallization will flow through the dielectric, creating a short. However, in some instances where there is particularly thin metallization, or there is sufficient energy passed through the short, the metal will vaporize and the short will clear. Degraded performance may result due to cratering left in the dielectric material but it may not constitute a catastrophic failure. It is possible that the short might reappear or performance may continue to deteriorate.

Table 1. ESD Failures in MOS Structures

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
MOS structures	1. MOS FET (discrete) 2. MOS ICs 3. Semiconductors with metallization crossovers (bi-polar and MOS digital ICs, bi-polar and MOS linear ICs) 4. MOS capacitors used in hybrids and linear ICs	Surface inversion or gate threshold voltage shifts from ions deposited on surface from ESD (charge injection into dielectric material	Operational degradation

Semiconductor Junctions

Semiconductor junctions that are susceptible to ESD damage include p-n junctions, p-i-n junctions, and Schottky barrier junctions. Their susceptibility to ESD depends on geometry, size, resistivity, impurities, junction capacitance, thermal impedance, reverse leakage current, and reverse breakdown voltage. Junctions with high breakdown voltage of greater than 100 volts and low leakage currents of less than 1 nanoampere are generally more susceptible to ESD than junctions of comparable size with low breakdown. Base-emitter junctions in integrated circuits and discrete bipolar transistors are typically more susceptible to ESD damage than base-collector or collector-emitter junctions. Junction Field Effect Transistors (JFETs) which have high impedance gates are particularly susceptible to ESD. Because these devices have very low gate to drain and gate to source leakage and relatively high breakdown voltage, the gate to drain and gate to source paths are usually the most ESD sensitive. Schottky barrier junctions, such as those employed in Transistor-Transistor Logic (TTL) Schottky integrated circuits, are especially ESD sensitive devices since they contain metal, which may be carried through the very thin junctions.

The temperature coefficient of extrinsic semiconductors is positive. Thus, the higher the temperature, the higher the resistance. As ESD events occur across the junction the temperature at the depletion region increases quickly and the extrinsic semiconductor material becomes an intrinsic semiconductor material, resulting in thermal secondary breakdown. It is possible for hot spots to develop but not grow completely across the junction such that at low bias voltages they do not cause a failure condition. However, during operation certain bias conditions, locally high current densities may exist with a corresponding large increase in temperature at the previously formed hot spot locations. Thus, growth of a filament short may continue or silicon and metallization may diffuse through the junction via the electromigration process at temperatures greater than + 200°C. The low leakage high breakdown JFET and

Schottky barrier junctions seem to be particularly susceptible to this failure process. With JFETs, highly localized currents can occur during junction reverse breakdown. With Schottky barrier junctions, metallization is immediately available to migrate through the junction at localized hot spots. As a current filament develops across a semiconductor junction, it essentially is putting a short across the junction. The failure indicator will be high leakage current.

Table 2. ESD Failures in Semiconductor Junctions

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Semiconductor junctions	1. Diodes (p-n, p-i-n, Schottky) 2. Bi-polar Transistors 3. JFETs 4. Thyristors 5. Linear and Digital Bi- Polar ICs 6. Input protection circuits on discrete MOS FETs and MOS ICs	Microdiffusion from microplasma - secondary breakdown from excess energy or heat Current filament growth by silicon and aluminum diffusion (electromigration)	Short circuit (no diode or transistor action)

Film Resistors

Thin as well as thick film resistors are frequently used in Hybrid microcircuits. Some Hybrid devices, such as precision voltage regulators, are sensitive to ESD because their designs do not tolerate large changes in resistance. Thin film resistors are energy dependent structures and do not have changes greater than five percent in resistance until the discharge energy is great enough to cause film rupture. Besides hybrid microcircuits, some monolithic microcircuits contain encapsulated thin film resistors (such as polysilicon resistors) as part of an input protection circuit. Resistance for thick film resistors are heavily dependent on voltages rather than energy and consist of a conductive metal oxide as the resistive element, a glass frit to provide a support matrix, a metal additive to enhance electrical performance, and substrate adhesion material. Since thick film resistors almost always experience negative resistance changes, electric discharge is considered as a possible trimming method when conventional trimming overshoots the desired resistance tolerance. Discrete encapsulated resistors, which contain the film resistor structure, are also ESD sensitive. Other resistor types that may be somewhat ESD sensitive include carbon film, metal film and metal oxide, especially ones at low tolerance and low wattage ratings. Putting these parts in a polyethylene bag and rubbing them against another bag would be enough to shift the tolerance of these resistors.

The failure indicator for thin film resistors due to ESD exposure is typically a shift in resistance. Generally, resistor stability is reduced as a result of ESD exposure and the degree of instability is directly related to the level of ESD exposure. For thick film resistors, the resistance shift is negative and this resistance change can easily exceed 50 percent with some thick film resistors. At low resistance values, however, there may be some exceptions to this. For other resistor types such as thin film, metal film, metal oxide and carbon film at lower ESD levels, small negative resistance shifts of less than five percent can be experienced. At higher ESD levels, large positive shifts greater than ten percent can be experienced, depending on the power rating.

Table 3. ESD Failures in Film Resistors

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Film Resistors	1. Hybrid ICs using thick and thin film resistors 2. Monolithic ICs using thin film resistors 3. Encapsulated film resistors	Dielectric breakdown, voltage dependent - creation of new current paths (for thick film only). Joule heating-energy dependent- destruction of small current paths (others)	Resistance shift

Metallization Strips

Metallization strips situated on substrates which are relatively thin and narrow and carry current between terminals without any other energy-absorbing element in the path are especially susceptible to ESD failure events. These metallization strips typically consist of aluminum or gold but can also be multi-layered. The common failure mechanism is burnout due to Joule heating. Metallization strips are often used in parts such as monolithic ICs, hybrid microcircuits, and multiple finger overlay transistor construction found in switching and high frequency transistors. Increasing the width or thickness of the strip will decrease ESD sensitivity. The use of glassivation and thinner SiO_2 regions between the strip and the silicon also reduces ESD sensitivity. The failure indicator from this type of failure is typically an open circuit.

Table 4. ESD Failures in Metallization Strips

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Metallization Strips	1. Hybrid ICs 2. Monolithic ICs 3. Multiple finger overlay transistors	Joule heating - energy dependent metallization burnout	Open Circuit

Passivated Field Effect Structures with Nonconductive Lids

Various NMOS and PMOS IC designs have been known to fail from very localized high concentrations of positively charged ions located on the outer passivated surface of the die. NMOS designs fail from excessive leakage currents from field inversion between N+ junctions such as thick field parasitic transistors, intermediate field parasitic transistors, EPROM transistors, and normal select transistors. PMOS designs such as the floating gate, EPROM, or depletion-type FET device fail when the negative charge on the floating gate is overcompensated by positive charge clusters on the outer surface of the die. This causes the part to “turn off”, resulting in an erroneous unprogrammed indication. Hermetic packages, which have recorded this failure mode, have non-conductive lids made from nontransparent ceramic, transparent sapphire and transparent borosilicate glass. It is possible to prevent these failures by grounding the bottom surface of the lid over the die or by being careful to avoid ESD incidences during handling of the device. This failure mechanism is most common with NMOS and PMOS UV EPROMs having transparent lids. Also, NMOS Static RAMs (SRAMs) contained within static packages have been known to fail from this particular ESD failure mechanism. It is also quite possible that LSI ICs with non-conductive lids could contain field effect structures, which are susceptible to failure from undesirable field inversion or gate threshold voltage shifting. The failure indicators for this type of failure mode come under the general classification of operational degradation, normally in the form of a function failure.

Table 5. ESD Failures in Passivated Field Effect Structures with Nonconductive Lids

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Field effect structures with non-conductive lids	1. LSI and memory ICs employing non-conductive quartz or ceramic package lids, especially ultraviolet (UV) EPROMs	Surface inversion or gate threshold voltage shifts from ions deposited on surface from ESD (charge injection into dielectric material)	Operational Degradation

Piezoelectric Crystals

Part types such as quartz crystal oscillators and surface acoustic wave (SAW) devices can fail from ESD events, usually resulting in operational degradation. In the case of piezoelectric crystals, the damage is caused by excessive driving current. The piezoelectric effect from high voltages causes mechanical stress and movement to be generated in the crystal plate. When voltage is excessive, mechanical forces cause in excess of the elastic limit of the crystal and crystal fracture occurs. Such fractures, when occurring in sufficient number, will cause enough change to the operating electrical characteristics to cause failure.

Table 6. ESD Failures in Piezoelectric Crystals

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Piezoelectric Crystals	1. Crystal Oscillators 2. Surface acoustic wave devices	Crystal fracture as a result of mechanical forces when excessive voltage is applied	Operational Degradation

Closely Spaced Electrodes

When using thick metallization such as 13,000 Angstroms, gaseous arc discharge in an arc gap 50 µm wide can be used as a protection device to dissipate incoming high voltage spikes.. For parts with closely spaced unpassivated thin electrodes, such as surface acoustic wave devices, high frequency multiple finger transistors, Very Large Scale Integration (VLSI) devices, and Very High Speed Integrated Circuits (VHSIC) devices, degradation from arc discharge can occur.

Table 7. ESD Failures in Closely Spaced Electrodes

Technology	Part Type(s)	Failure Mechanism	Failure Indicator
Closely spaced electrodes	1. Thin metal unpassivated, unprotected semiconductors, microcircuits and surface acoustic wave devices	Arc discharge, melting and fusing of electrode metal	Operational Degradation

GaAs-Based Components

The silicon semiconductor industry has experienced field failures and yield losses as a result of ESD events. Unfortunately, very little research has addressed ways to design and fabricate protection circuitry to increase the static damage threshold of compound semiconductor devices, such as those manufactured using Gallium Arsenide (GaAs). It is well known that many of these semiconductors are extremely sensitive to ESD events, compared to their silicon counterparts. Numerous ESD-induced failures have been reported in military and commercial system applications. Current GaAs devices often possess low ESD-failure thresholds, and anticipate the next generation of GaAs-based components will be even more ESD-sensitive, due to smaller lateral dimensions, low melting point substrates, the implementation of deposited passivation layers, the use of non-planar semiconductor surfaces, and the implementation of reverse-biased circuitry.

Table 8. ESD Failures in GaAs-Based Components

GaAs-Based Component Description	ESD-Induced Failure Indicator
Bipolar Transistor	Decrease in bipolar transistor beta
Field Effect Transistor (FET)	Decrease in FET transconductance Increase in gate leakage current FET gate open circuit FET gate-source short circuit
Various	Increase in noise figure
Various	Open in interconnect metallization
Various	Catastrophic electrical failure
Various	Physical damage to device or circuitry is visible, possibly catastrophic

Today, many GaAs MMIC device manufacturers are implementing protection networks on their chips as a preventive measure for ESD events. A common practice for accomplishing this is the placement of “clamps” between the bonding pads and the corresponding MESFET gate to which the pad is ultimately connected. The common protection elements for these ESD protection networks include diodes, resistors, contacts between metallization and diffused regions, metallization, three layer devices (n-p-n or p-n-p), and four layer devices (p-n-p-n). In the case of a typical MMIC device ESD clamp, the protective circuitry may consist of two current-limiting resistors and two Schottky diodes. Protection networks can be successfully used on power supply pins, control inputs, and some digital circuitry. Networks designed for high frequency applications should be carefully designed into the original circuit. Recommend pad clamps be included as an integral part of the MMIC protection network ensemble. The protection circuit components can be selected and the corresponding chip can be tuned to account for any additional impedance, which may be present in the protection networks. The military handbook MIL-HDBK-263 is an excellent resource in providing guidance and considerations for the design and implementation of ESD protection networks in electronic devices.

ESD precautions must extend to the mounting and lead soldering of packaged FETs, and it is important to ensure that all soldering equipment is securely grounded. The attachment method for packaged FETs and MMICs must take into account the potential for mechanical damage to the electrical leads and/or the hermetic seal of the package. The position of the package must not be altered once lead detachment begins. Hand soldering is recommended for electrical leads and should be performed at a temperature of 650 C or less with maximum heating time of two seconds per lead. For stripline type packages, the source leads should be soldered first followed by the drain and gate lead, in that order.

ESD PRECAUTIONS

Of all the yield losses the user is likely to encounter in the handling of silicon and GaAs FETs and MMICs, damage due to electrostatic discharge is a major cause. This is generally the case, regardless of where the yield loss may appear in the assembly process. An insidious form of electrostatic discharge damage in GaAs FETs, which could be called ESD "pre-kill", occurs when the level of damage, though insufficient to produce outright failure, causes changes in the substrate or the metallization which will eventually result in failure of the device at a later assembly step or in the Field. A common form of this "pre-kill" phenomenon results from an electrostatic discharge to the device which is sufficient to vaporize GaAs in the active channel area, weakening the device's ability to withstand electric field, current flow and/or temperature. If the area of vaporization is extensive or near the surface, "cratering" can sometimes be observed.

With this background, the following ESD control measures are recommended in the handling of silicon or GaAs devices:

a. Establish a reliable earth grounds for all tables, die detach stations and wire bonders. Cold water lines and the ground lug of a 3-wire electrical outlets are inadequate and even a copper rod (driven through the floor) may not be adequate in some soil conditions. Proper grounding of wire bonders must include grounding of the tool itself.

b. Require the use of wrist grounding strap for every handling operation, starting with removal of the shipping containers from the metallized bag. Since the effectiveness of the wrist strap is the important point, not the wearing of it, wrist strap test stations should be installed and their use required.

c. Require all operators to wear ESD control smocks that use conductive threads.

d. Use ionizing blowers at all work stations.

e. Measure relative humidity at the start of each work shift, and observe the guidelines for minimum humidity levels for various operations. Install humidifiers, if necessary, to continue operations during periods of low humidity.

f. Use conductive surfaces and floor mats where appropriate.