RAD Hard Selection Process for RHA Devices as an Element of Design

Scope

This section provides a suggested process for selecting microcircuits with the required performance, reliability and radiation hardness capabilities. The goal of this process is to ensure cost effective designs that satisfy all of the above noted requirements.

General Process

The parts selection process, as in the non-radiation environment situation, must begin with a clear understanding of the application, including both the electrical performance required and the application environment (e.g. temperature, atmosphere, vibration, etc.). However, for device applications in systems that must operate and survive in a radiation environment, these radiation effects must be superimposed upon the other natural environment conditions.

This latter task is especially significant since the effects of the ambient environment (e.g. temperature, atmosphere, etc.) will impact the radiation response of the microcircuits.

Radiation Response Variability

One of the major issues concerning the use of microelectronics for applications which require radiation hardness is the variability of the radiation response of a specific technology and the designs emanating from that technology.

Two specific issues must be considered:

(1) The sensitivity of the response of a circuit to a particular environment or failure mode (e.g., total ionizing dose, dose-rate, SEE, displacement damage, etc.) due to otherwise acceptable process variations.

(2) The statistical process controls (SPC) and qualification conformance inspection (QCI) procedures used by a specific semiconductor supplier to maintain critical process/design parameters for radiation hardness.

In general total ionizing dose response is the most sensitive of the radiation effects to processing parameters. The processing parameter associated with gate oxide and field oxide growth are the most critical. Moreover, relatively small changes in processing temperature, time, pressure, contamination, and atmosphere (e.g., argon vs. nitrogen; steam vs. dry) can have a dramatic effect

on final process robustness. Circuit design rules and layout also are important, but not to the same degree as processing parameters.

Dose-rate upset, SEE and displacement damage are more affected by piecepart electrical design rules and layout than the process parameters. However, individual transistor response (e.g., current drive and propagation delay) plays an important role concerning dose-rate and SEE response.

In general, total ionizing dose affects both MOS and bipolar technologies; dose-rate upset and SEE affect MOS, bipolar and GaAs technologies and neutron/proton irradiation (displacement damage) affects bipolar technology and MOS technologies associated with electro-optical devices (e.g., charge-coupled and charge-integrating devices).

Concerning semiconductor supplier SPC and QCI, the following can be stated:

· QML Suppliers with specified RHACL's: For these suppliers the radiation sensitive process and design parameters have been identified and kept under strict control. Consequently, minimal variability in circuit (technology) response is the standard.

· RHA Suppliers: These suppliers are typified by the application of stringent post-fabrication screening and characterization procedures as a method of supplying in-specification products. These suppliers may or may not have identified all critical processing/design parameters, since post-fabrication screening is relied upon to meet specifications. Hence, in some cases, greater variability in radiation response can be anticipated and precautions should be taken to ensure that circuit performance is not compromised when using these circuits.

· Non-RHA/QML Suppliers: Products provided by these suppliers can be anticipated to have significant variability concerning their radiation response. Hence, stringent characterization, screening and testing is mandatory.

The subsection on Radiation Hardness Assurance in the section on Selection Guidance provides additional discussion concerning the RHA procedures required for the different classes of semiconductor suppliers.

Application Specific Integrated Circuits (ASICs)

The use of ASICs in a radiation environment provides a number of unique challenges for a circuit designer. This occurs since, in addition to the standard effects on radiation response caused by process and design variations, specific personalizations can also impact radiation hardness capability.

Thus, although a robust set of process and design rules may be available for a QML manufacturer, it still may be necessary to perform radiation testing on every personalization of a gate array.

The requirement to perform testing for specific environments and the complexity of the testing will depend on the margin between the radiation levels of the operating environment and the capability of the technology.

The need for the testing is, as previously stated, due to the effects the layout, physical interconnections, and the die have on the radiation hardness of a specific ASIC. In the following discussion each of the radiation environments will be discussed.

(1) Total Ionizing Dose: The effects of TID in an MOS circuit are in general to reduce operating speed, increase leakage current, reduce individual transistor current drive, and reduce transconductance. Concerning these effects, leakage current and operating speed must be dealt with by the basic process and layout rules.

However, to ensure satisfactory IC operation circuit design rules that govern transistor fan-in and fan-out, signal and clock routing, etc. must be considered.

Depending on the design margin, changes in transistor operating speed can result in "race" conditions for specific personalizations.

In general, simulation and analysis can be used to identify and investigate worst-case signal paths, and based on the design margins, a decision to perform total ionizing dose testing for a specific personalization determined.

(2) Dose-Rate-Upset/Survivability: There are two specific issues which strongly suggest that each individual personalization be subjected to dose-rate upset testing. These issues include:

· The effects of the die power distribution on the upset level of circuits interior to the die. Circuits which are furthest from the input power pins suffer the greatest IR (voltage) drop caused by the dose-rate engendered photocurrents and will be more prone to upset due to rail-span collapse. Thus, these sensitive areas must be identified to ensure worst-case testing.

· The effects of transistor location on charge collection. The proximity of a transistor or circuit to the edge of a die or to other transistors can significantly affect the amount of photocurrent collected at critical junctions/nodes.

In addition, circuit design rules concerning fan-out/fan-in and I/O loading can also influence upset levels both at internal nodes and at the outputs.

Thus, the dose-rate upset performance of a complex ASIC can be significantly affected by the actual layout of the transistors which comprise that circuit.

The sensitivity of the ASIC to layout will of course be a function of the performance capability of the process/design to the actual threat level or the so-called design margin.

Here again, the need to perform comprehensive testing can be identified through analysis and simulation. However, the issues of identifying sensitive areas of a die and the input vector set required to exercise those sections of the circuit personalization greatly increase the difficulty associated with both simulation and testing.

Proprietary simulation codes exist (e.g., BUSNET, a product of Mission Research Corporation) to accomplish this type of analysis and should be used to support any dose-rate upset testing. Also, for testing of this complexity, pretest analysis is mandatory to ensure worst-case situations are accurately identified.

(3) Single-Event-Effects: Specific ASIC personalizations can also affect SEE performance and complicate establishing a simple quantifiable metric (e.g., errors per bit/day for a memory) for a particular design.

Some of the factors that would influence the SEE performance include:

· The specific operation (i.e., input excitation vectors, and mode of operation, etc) of the circuit in progress at the time of the ion strike will determine the nature of the single event effect. The complexity of this factor can be appreciated if we consider the SEE sensitivity of a microprocessor such as a 486. The specific operation in progress, the data being operated-on, etc. will all affect the overall IC response.

· The propagation path of an upset. Specifically, a heavy ion strike can result in the creation of a spurious signal at some location in a combinatorial circuit. This signal or glitch can propagate through the circuit until it is attenuated to a level where the signal is no longer capable of causing an upset or until it reaches (i) an output pin and propagates off chip with to-be-determined consequences or (ii) reaches an internal latch with sufficient amplitude and duration to reset the circuit. Once "latched" this spurious signal will then be interpreted as a "real" signal with TBD consequences.

Here again the basic concerns are somewhat similar to those engendered by dose-rate upset with the exception that the spurious signal is local rather than global. Also, the same type of simulation methods can be used to determine worst-case situations.

In addition, non-nuclear types of testing such as laser probing can be used to identify sensitive areas within a die and worst-case conditions (e.g., bias voltage, input vector, mode of operation, etc.).

Thus, for certain critical ASICs, a comprehensive analysis and test qualification program is required to support operation in a radiation environment (e.g., space, etc.). The level of detail and completeness of these tasks will be governed by the technology design margin and criticality of the application.

Radiation Hardness Considerations

Proper application of microcircuits requires a thorough understanding of the radiation environment, the system functions which must be performed and the hardness of the semiconductor devices which are available.

The effects of radiation on various semiconductor technologies is summarized in Table 1.

The specific radiation environments as a function of device application are summarized in Table 2.

Finally, Table 3 provides a summary of threat environments vs. threat mitigation methods.

In general, device design margin can be traded-off against considerations such as shielding, circuit and system design complexity (e.g., circumvention, EDAC, voting, etc.), RHA requirements (e.g., lot testing, individual device screening, etc.) and overall system design complexity. Obviously, the "best" solution is the one which simultaneously achieves the required system performance (including reliability or MTBF) and minimizes total cost of ownership.

Table 1. Radiation Effects on Semiconductor Technologies.

Category	Cause(s)	Mechanism	Effect
Total Ionizing Dose Irradiation	Natural Environment: Trapped electrons and protons in the earth's magnetosphere	Charge buildup in the oxide and other materials used to fabricate semiconductor devices	Metal Oxide Semiconductor (MOS): - Increased leakage current - Changes in operating speed - Parametric and functional failures Bipolar Transistors: - Reduced gain - Increased leakage current

	NWE: XRays gammaRays		- Parametric and functional failures GaAs: - Insensitive FO and EO: - Increased attenuation
Single-Event-Effects	Natural: Galactic CosmicRays Solar Enhanced Particles Energetic protons and neutrons NWE: Energetic neutrons	- Deposition of charge insemiconductor devices through impact of protons or ofheavy ions from GCRs - Nuclear Reactions caused by protons and neutrons	MOSs: - Upset - Burnout - Gate rupture - Latchup Bipolar: - Upset - Burnout - Latchup EO: - Increased CCD dark current Solar Cells: - Degradation in efficiency GaAs: - Upset
Displacement Damage	Natural: Energetic protons and Neutrons NWE: Neutrons	- Lattice Damage in semiconductor Material resulting in trap formation and doping compensation	FO and EOs: - Increased attenuation - Loss of efficiency (CTE) -Increased dark current Solar Cells: - Loss of efficiency GaAs: - Gain Degradation FET (Si & GaAs): - Relatively Insensitive Bipolar (Si): - Power & low f_t devices more sensitive -Gain reduction and an increase in bulk Si resistance
Dose-Rate	Prompt Radiation: Gamma rays X rays	Photocurrent generation	MOS, Bipolar & GaAs: - Upset - Burnout - Latchup FO & EO: - Darkening - Upset

TABLE 2. Application/Threat vs. Device Requirements.

Application	Threat Environment	Representative Device Requirements
ICBM & Strategic Interceptor	• Primary: - Neutron Irradiation - Dose-Rate - upset/Survivability • Secondary - Total Ionizing Dose	• Neutron Irradiation >10^{13} n/cm 2 • Dose-Rates > 10^{8} rad/s • Total Dose < 10 krad(Si)
Military Surveillance, Navigation & Communications Satellites (GEO & 1/2 GEO) (Natural & NWE)	• Primary - Total Dose - SEE - Dose-Rate-Upset • Secondary - Displacement Damage (neutrons & protons)	• Total Dose ³ 300 Krad(Si) • SEE < 10 -10 errors/bit-day • Dose-Rate < 10^{8} rad/s • Neutrons < 10^{12} n/cm 2
Commercial Communications Monitoring Satellites (natural & NWE)	• Primary - SEE - Total Dose (NWE) • Secondary - Total Dose (natural) - Displacement Damage (protons/neutrons)	• SEE < 10^{-9} errors/bit-dag • Total Dose ~ 30 krad(Si) NWE (LEO) ~ 10 krad(Si) Natural
Tactical Military Systems Including Avionics	• Primary - - Dose-rate (upset & Latchup) - SEE (for avionics)	• Dose-Rate: 10^{9} rad/sec • Neutron irradiation: 10^{12} n/cm^{2} • Total Dose: < 5krad(Si) • SEE: < 10^{-9} errors/bit-day

	• Secondary - Total dose - - Neutron irradiation	
Nuclear Reactor Control & Scientific Systems	• Primary: - Neutron irradiation - Total dose	• Neutron irradiation: > 10^{13} n/cm 2 • Total dose: > 100 krad(Si)

TABLE 3. Threat Environment vs. Mitigation Method.

Threat Environment	Mitigation Methods
• Total Ionizing Dose	• RH Parts • Shielding - Note that for high energy electrons & proton environments shielding is minimally effectivedue to bremsstrahlung effects • Circuit Design - Bias for max. gain
• SEE - Upset - Latchup - Gate Rupture - Burnout	• RH Parts (design, layout & material) • Shielding for protons & neutrons only • System Design - EDAC, voting, etc.
• Dose-Rate Upset & Survivability	• RH Parts • Shielding – shield X-Ray to gamma limit • Subsystem Design - Circumvention - Power Strobing - Operate-thru
• Displacement Damage - NWE (Neutrons) - Natural (protons & neutrons)	• RH Parts (high ft Bipolar transistors or FET technology)

	• Shielding – for protons • Circuit Design - bias for minimum neutron degradation