DEVELOPING TECHNOLOGIES
(MICROELECTRONIC COMPONENTS AND MATERIALS)

INTRODUCTION

Developing technologies discussed here are not necessarily brand new technologies. Some are, some have been around for years, most have been known to exist for some time. The common denominator is that they now seem to be, or will soon be, a viable commodity ready for marketing. For example, Silicon/Germanium has been around for years and Copper interconnects have been desirable since the beginning. It has been only recently that each of these processes has become viable to the point of producibility through technology development. The intent here is to provide the latest information in significant detail as it might affect the use of the technology in today's designs both new or updated.

For the purpose of this document, a product or process is considered a candidate as a developing technology if it qualifies to one or more of the following attributes that are beyond the current technologies being marketed: faster, smaller, lighter, cooler, higher power, higher/lower operating temperature, lower/higher voltage, lower noise level, and most of all, affordable.

PROSPECTIVE PRODUCT, PROCESSES AND MATERIALS

This document presents new, and possibly unfamiliar, concepts in materials, processes, and products. The following is a list of materials that may be encountered during subsequent investigations into specific items of interest and is intended to briefly provide some additional insight.

Semiconductor/Active Materials

Bismuth Telluride (Bi_2Te_3) -- primarily a thermo electric material.
Boron (B) -- very suitable as a thermistor material.
Cadmium Sulfide (CdS) -- popular in photo, optical, and solar cell applications.
Diamond (crystalline C) -- poor S/C, however, excellent thermal conductivity, electrical. insulation, optical transmission and high temperature properties (see Diamond).
Gallium Arsenide (GaAs) -- microwave applications (see Microcircuits and Hybrids/MCMs).
Gallium Nitride (GaN, GaAlN) -- focal plane array detectors (UV solar-blind applications).
Gallium Phosphide (GaP) -- high temp./ high freq. devices (see GaP).
Germanium (Ge) -- early microwave diode and first transistors (see SiGe).
Gray Tin (crystalline Sn) -- semiconductor, no known appreciable usage.
Indium Antimonide (InSb) -- photovoltaic, magnetoresistive (e.g. flux meters) applications.

Indium Phosphide (InP) -- early high speed, optical substrates and InP based microwave ICs.
Lead Sulfide (PbS) -- early RF detectors, now as infrared detectors.
Mercury/Cadmium/Telluride (HgCdTe) -- focal plane array det. (lrg Si or Sapphire wafers).
Platinum Silicide (PtSi) -- low noise, high sensitivity imaging focal plane arrays.
Selenium (Se) -- early rectifiers and photoconductive applications.
Silicon (Si) -- most common semiconductor (see appropriate sections).
Silicon Carbide (SiC) -- varistors, high temperature devices (see SiC).
Tellurium (Te) -- seldom as a transistor, mostly as constituent in various S/C compounds.
Thallium (Tl) -- Thallium based materials for IR detectors.

Fabrication Materials

Substrates and Insulators:

Alumina (Al_2O_3) -- substrate for multiple usage, general purpose devices.
Aluminum Nitride (AlN) -- high temperature applications (see AlN).
Beryllia (BeO) -- good heat dissipation substrate for power device applications.
Cofired Ceramic (Al_2O_3 multilayered) -- multilayered/interconnected circuit applications.
Diamond (crystalline C) -- good electrical insulator (see Diamond).
Ferrite (Fe_2O_3) -- microwave/magnetic applications e.g. circulators.
Glasses (variety of compositions, e.g. Al_2O_3 , Na_2O, SiO_2 , etc.) -- displays and multiple uses.
Glazed metal (porcelain-enameled) -- specially shaped and large substrates.
Nitrides (BN and Si_2N_4) -- Hi-temp electrical insulators, excellent at room temperature.
Organic (variety of polymerics, e.g. polyesters, polycarbonates, polyimides etc.) -- low cost/low temp. applications (flex circuits, multilayered substrates, membrane switches, etc.
Quartz (fused silica as high purity SiO_2) -- microwave device substrate applications.
Sapphire (the single-crystal form of Al_2O_3) -- for smooth surface substrate applications.

Conductive Metallization, Deposition Barriers and Platings:

Aluminum (Al) -- conductor for electronic components (see appropriate sections).
Copper (Cu) -- replacing Al as primary conductive metal (see appropriate sections).
Gold (Au) -- interconnect wires, wire bonds, and protective platings.

Kovar (Fe/Co/Ni alloy) -- leadframes, leads, reinforcement and matrix applications.
Molybdenum (Mo) -- higher conductivity barrier metal and promotes adhesion.
Nickel (Ni) -- barrier metal under conductive metals and protective platings.
Nitrides (TiN, ZrN, TaN and HfN) -- stable-effective barrier layer between Al and Si/Silicides.
Silicides (WSi_2, $MoSi_2$, and $TaSi_2$) -- enhance hi-temp stability processing of substrates.
Titanium (Ti, Ti-W) -- used as barrier metals, promote adhesion.
Tungsten (W) -- higher conductive. barrier metal, promotes adhesion, multilayer substrates.

PACKAGING/INTERCONNECTS

The technologies discussed here greatly enhance PCB performance and will be a significant percentage of marketable product within this decade. The push for highly sophisticated products with higher power capabilities, more I/0s, and faster speeds has generated demands for very high lead count, reliable advanced package designs. The most recent technologies covered in the following paragraphs consist of three basic concepts:

Leadframe Technologies, Medium to High I/O Counts

In all leadframe designs, die is mounted to an adhesive securing it for wire bonding with Au wire (Al may also be used). This provides the die-to-leadframe electrical connection. The package is completed by encapsulating the die-leadframe assembly with a plastic molding compound for protection. The major advantage of the leadframe design is package flexibility, which accommodates some differences in thermal expansion between the package and PCB.

Ball Grid Array Technologies (BGA)

Typically, ball grid array technologies are smaller pin-for-pin than leaded devices, tend to be much more robust than leaded devices, and are not as easily damaged during handling and assembly. They are an attractive device, because of the ease of attachment to the PCB. However, array devices have the solder interconnects located under the package, which makes visual inspection difficult. Also, multilayer PCBs, with a distribution layer connected to the inner solder joints of the array device and plated vias, are required to provide signal escape routing between the solder sphere mounting pads. This increases board costs.

Direct Chip Attach (DCA)

DCA technologies involve attaching the die directly to the PCB. These technologies offer an increase in high-speed performance and a significant reduction in real estate; however, sophisticated and specialized assembly processes are required.

The two most popular direct chip attachment types are flip-chip (FC) and chip-on-board (COB); each technology has several variations:

Flip-Chip

The first successful flip chip process was created 20 years ago as the “C4 process” (controlled collapsible chip connection). Flip-chip features a die with a bump-like attachment provision (usually eutectic, high-lead solder) bonded to what would be wire bond pads in past designs, and then, these are usually attached directly to the PCB or a flex circuit (referred to as FCOB), and sometimes are attached directly to a package (e.g. MCMs). There are several other metallurgical bump materials available e.g., high temperature solder, Ni/Au , and electrically conductive adhesives. Electrically conductive polymer adhesive bumping is gaining popularity as it has some advantages over traditional solder. Polymer bumping allows lower temperature processing, permitting a wider variety of substrate and board materials, and is less susceptible to thermal fatigue. Once attached, a dispenser deposits underfill around one or two sides of the flip-chip for added mechanical strength to the die interface bond. Flip-chip technology has performance and real estate advantages including reduced inductance and increased performance at higher frequencies. Disadvantages include special attachment processes, extreme CTE mismatches between the die and substrates, and there is a significant increase in the difficulty of testing the die at the assembly level.

Chip-on-Board

Chip-on-board (COB) processing (attaching the IC die directly to the PCB) is accomplished much like attaching to a standard leadframe. Advantages include a great reduction in board real estate, higher circuit performance, and the ability to process the chip with traditional semiconductor methods. The die to PCB attachment adhesive contains silver flakes for thermal conductivity. For electrical connections, the die is wire bonded to the board with a gold-to-aluminum bond at the die, and a gold-to-gold bond on the board. Environmental protection of the die is normally accomplished with some method of coating over the die, e.g. a silicone glob. Disadvantages include the need for specialized processes, materials, high-purity wire bondable gold pads on the PCB, and “Known Good Die (KGD)”.

Wafer Level Glass Shell

Wafer level glass shell is for ultra-thin applications (like Smart Cards) and consists of sandwiching a thinned die between two glass plates, or for high heat dissipation applications, aluminum nitride plates (see diagram below). The lapped wafer is encapsulated, the I/O pads are exposed and metallization applied to make the I/O connections. This technique, by encapsulating the die before singulating into a package (not much larger than the die), provides protection during subsequent handling of the die. Other advantages include increased speed, improved resistance to parasitics, ease in

heat sinking, and it can be attached with conventional soldering rather than TAB or wire bonding. Another practical attribute is its resistance to opening without destroying the chip, thereby eliminating the illegal reverse engineering possibility on a stolen Smart Card. It is also a candidate as replacement for direct chip attach designs.

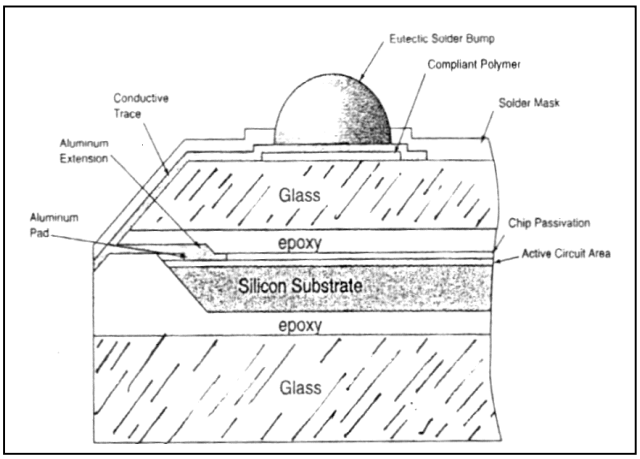

Figure 1. Wafer Level Glass Shell

PROCESSES

The following discussions pertain to those processes that are new, altered, or under development to achieve a desired improvement in the associated materials characteristic and/or product performance.

Copper Metallization

The use of copper is quickly becoming widespread, as the inherent advantages are too significant to ignore. Copper has the potential to reduce overall resistivity, capacitance, power consumption, transition times, and metal levels. Each of these is a significant advantage for producing smaller and faster devices; and copper has better resistance to electromigration, which is a significant problem with aluminum. Recent advances employing an inlay technique called the Damascene Process (A process similar to ancient decorative process used to make Damascus steel swords.) has brought copper forth as the preference over the traditional aluminum metallization. The inlay process will incorporate a nitride diffusion barrier of tantalum or titanium to prevent poisoning of the silicon. Interestingly, it has been determined that a uniform barrier thickness on the bottom and sides of the inlay trench is not as critical as the grain structure in preventing unwanted voids. A seed layer of copper will be added over the nitride barrier. The final copper layer, bulk application, will be traditional electroplating; however, this must be followed by CMP (chemical-mechanical polishing) to achieve surface co-planarity, a difficult step because of considerable variation in material hardness.

SiGe Die

Although silicon remains the predominant semiconductor material and gallium arsenide is used for high frequency applications because of its higher electron velocity, silicon germanium has been of significant interest since it was first proposed in 1957. SiGe may become a viable alternate in the near future as the critical process step of low temperature, SiGe epitaxy has been successfully developed using a patented ultra-high vapor deposition (UHD-CVD) epitaxial reactor. Like GaAs, SiGe has a high velocity electron characteristic (23 Gigahertz operation) but operates cooler, is 25 % cheaper and is easier to produce as it can be fabricated in a standard silicon chip factory. SiGe disadvantages are lower breakdown voltage and greater susceptibility to crosstalk problems than GaAs.

Lithography (Post Optical Methods)

Although optical lithography has the capability to produce sub-0.10 micron features, it has been accomplished only in a research project. Extreme ultraviolet (EUV) technology has been attracting the most attention . It is a step beyond deep ultraviolet (DUV) and still in the X-ray spectrum. It is referred to as “soft X-ray” denoting its place outside the visible/invisible spectrum of light. There are three non-optical lithography processes under serious development: proximity X-ray, projection E-beam, and EUV. Ion-beam projection lithography (IPL) and electron beam direct write methods are still being developed by some organizations. However, EUV now seems to be the US industry preference, while IPL is still very popular with the European community.

Microvias

The fourth generation of PCB technology is here. Initially it was single sided, copper etched track, followed by double sided with drilled, plated through holes, and then stacking the double sided boards with drilled holes through all layers; and, today’s 4th generation is blind and buried microvias.

Microvia Fabrication

The three microvia fabrication technologies used today are laser ablation, plasma etching, and photo defined processing.

a. The laser ablation technique is accomplished either by direct high energy ablation of the copper foil, followed by low energy ablation of the dielectric, where the next copper layer limits the ablation process, or by chemical etching the copper foil and using only low energy laser drilling of the dielectric.

b. The plasma etching process first requires the copper foil be chemically etched to reveal the dielectric. Then the dielectric is exposed to a plasma flield* consisting of

an oxidizing and fluorine gas which converts the dielectric material into volatiles for venting. The optimal gas mixtures depend on the material to be etched. The etching process is achieved in a vacuum chamber with a RF source providing the ignition energy. The copper, unaffected by the plasma, acts as a mask.

*Note: Plasma is a highly excited state of matter, often a diluted mixture of O_2, CF_4, and N_2 gases whose atoms and molecules are ionized and split to form highly reactive gas radicals.

c. The Photo defined process forms vias by printing and developing an image in a photo definable dielectric layer, which is applied by curtain coating, dry film lamination, or screen printing. The ensuing photo developing process removes the dielectric material at the via site creating the via and exposing the inner layer capture pad. Electroless copper plating is then employed to cover the surface of the dielectric. Laminate photo resist and print to develop the outer layer, and then the copper pattern is electroplated.

Advantages

Microvia technology greatly reduces real estate, increases high frequency performance, and reduces crosstalk and interference. These are accomplished by eliminating fanouts, reducing signal paths, and providing for construction designs that reduce inductance, capacitance and ground loops. Incorporating microvias in pads can produce savings up to 500% in board space.

Reliability Issues

All three processes are somewhat prone to degradation after solder reflow and under thermal shock and temperature cycling test conditions. An industry used solder reflow condition is considered a one-minute exposure to a temperature between +183^{o}C and +225^{o}C. Suggested industry used test temperature cycles/ranges are: Thermal Shock (up to 2000 cycles of liquid to liquid at –55^{o}C to +125^{o}C) and, Temperature Cycling (up to 1000 cycles at –40^{o}C to +125^{o}C). The degradation concern is with increases in via resistance above 10%, cracks in the via walls and, of course, electrical opens in the vias.

Flex Circuits

Although a product in it itself, flex circuits are also used as an interposer for redistributing the routing of the die pads to a configuration compatible with an existing technology. In this sense, it is part of an assembly process that provides a variety of interconnection possibilities for either rigid or flexible. hardware designs. The flex circuit is an attractive substrate material for 3-D MCMs because of its mechanical flexibility, low dielectric constant, high electrical resistivity and low cost. In addition, the same flex circuit design can be used with a stiffener to convert it to a rigid interposer when the application calls for additional strength and flatness in lieu of flexibility. However, since

polyimide flex has a low thermal conductivity, 3-D packaging does not allow a conventional heat sink, new, and novel heat management concepts need to be pursued.

3-D HDI

3-D HDI is a very efficient high density interconnect process, saving board space up to 70%. To achieve a reliable, cost effective end product, implementation of some or all of the following new technologies are required: KGD, flex circuit interposers, microvias, heat spreaders, embedded die, flip-chip attachment, and because conventional heat sinks cannot be used, non-conventional heat management methods need to be considered, e.g. diamond coated heat spreaders. Basically, 3-D HDI design entails the stacking of substrates with circuitry (die and metallization) into a multi-layered, multichip module. Electrical connections between layers may be accomplished at the edges or by vertical through holes/vias. KGD is normally used because being embedded in the assembly, chips are virtually inaccessible. The layers may each require the insertion of a heat spreader to provide a thermal conductive path out to the sides of the assembly for the die generated heat.. Usually a cooling process is provided at two opposite sides of the assembly (heat spreader outlets) while the I/Os are brought out at the other two sides. The cooling may be provided by circulating water heat sinks for high power applications to forced or air convection cooling depending upon the power levels involved.

Spherical Silicon Processing Technology

Spherical silicon processing technology is a non-contact process that uses inductively coupled plasma and fluid mechanics up to the placement of solder balls on the finished sphere. The process requires single-crystal spherical formation, non-contact handling, spherical lithography, 3-dimensional design, and clustering. Packaging is a layer of encapsulation simply referred to as “paint”. This process results in a silicon sphere that is robust in high temperature processing (up to +1300°C) and is virtually free from oxygen contamination potentially enhancing device performance. A typical device, e.g. a 16-bit multiplexer, could consist of three spheres (one control and two registers) in a 3-dimensional cluster. Development of 1-mm diameter spheres is underway, with smaller sizes as a future goal. Since there is no requirement for a clean room or vacuum equipment, processing costs are reduced making it potentially attractive to manufacturers.

Silicon-on-Insulator (SOI) Wafer Processing

Already in limited production, SOI is being considered a viable commercial process for the near future. SOI chips can require as little as one-third the power of presently produced microchips, which is a significant advantage for portable/mobile/wireless, battery powered applications. This advantage comes from the reduced operating voltage requirement of SOI product over conventional devices. Another SOI advantage is the reduction in soft-error rate, the upset of memory data

from cosmic and background radiation. Early use of SOI product has been in memory devices for space applications.

ELECTRONIC/OPTICAL PRODUCTS

Microwave Products

High frequency devices/materials are constantly under development as today's (and tomorrow's) communication and navigation requirements by both industry and government continually push the state-of-the-art product for faster, smaller, higher temperature, more rugged, but affordable microwave systems. The developing technologies of most interest to users of microwave products are GaAS*,* SiGe, GaP, InP semiconductors, and the low-loss dielectric materials for substrates and insulation. Significant aspects of these items are discussed in this document under the appropriate topics.

High Temperature Products and Related Materials

For purposes of discussion herein, high temperature products/materials are those which can routinely perform reliably over design lifetimes, at temperatures above 125°C and up to ≅ 1000°C. Temperatures of this magnitude preclude the use of typical hermetically sealed Ge, Si and GaAs devices, which are normally operated well below 200°C, and plastic encapsulants, which routinely have a glass transition temperature below 159°C. This discussion does not include those products that are designed to function only briefly at an elevated temperature, e.g. an immersion thermocouple used to measure the temperature of molten metals.

SiC as a Semiconductor

Because of its intrinsic refractory characteristics (working temperature of 1700°C in an oxidizing atmosphere) as a SiC-based distributed control electronics device, SiC devices could eliminate up to 90% of the wiring and connectors presently needed in conventionally sheltered systems applications e.g. aircraft engine compartments. In addition, in non-hot areas, SiC devices without cooling could reduce the weight and significantly improve reliability. In its nonlinear electrical grade, SiC has been a popular choice for varistors, power diodes and rectifiers. SiC has several advantages over both Si and GaAs for power devices that include a higher breakdown field, higher thermal conductivity, and higher radiation hardness. Because of its different polytypes with different electric properties, but compatible chemical structure, SiC offers a base for new generations of hetrojunction devices. An example is the n-p hetrojunction *of* GaN/6H-SiC with zero micropiping. Micropiping of the SiC is a processing problem and adding a layer of GaN to eliminate micropiping is one of the techniques under study in the development of high power-high temperature SiC devices.

Diamond

Rarely found in the Type II class where it behaves as a semiconductor (but poorly when compared to conventional silicon and germanium), diamond has not yet been marketed commercially. However, the Type I class with good electrical insulating characteristics and excellent thermal conductivity is readily available in sheets as polycrystalline diamond. Diamond has the highest thermal conductivity of all known materials, four to eight times higher than other heat conducting materials, e.g. Cu, BeO and AlN. Polycrystalline diamond sheets are produced by CVD (chemical vapor deposition), and are becoming a favorite choice as a heat-conducting layer between power devices and heat sinks serving as a heat spreader. The efficiency of heat removal from high microcircuit densities is critical, as they tend to generate higher junction temperatures; therefore, polycrystalline diamond is also a good choice as a substrate layer in Hybrid and MCM designs. The relatively low dielectric constant of diamond compared to other electrical insulating materials also makes it an attractive choice for high-speed MCM applications. After chemical polishing, circuit metallization of the diamond sheets with conventional photolithography techniques is possible, and either Si or GaAs die may be incorporated with polycrystalline diamond with minimal thermal coefficient of expansion (TCE) concerns.

AlN

To enhance operation of Si-based power devices for high temperature-high density applications (temperatures $\cong$ 200°C), a standard Si die can be sandwiched between two AlN plates. This process affords the advantages of the glass shell process but with a significant increase in high temperature capability. In addition, for applications with rapid, extreme temperature deviations, AlN exhibits good thermal shock resistance because of its high thermal conductivity and low TCE. The chemical inertness of AlN provides the stability characteristic required for processing at very high temperatures (900°C in oxidizing and 1600°C in reducing atmospheres). AlN is also a better candidate for the protective coating of large Silicon die, and as a substrate material for silicon and GaAs die. This is because of its high thermal conductivity, its good dielectric properties, and its closer TCE match to Silicon and GaAs than either SiC or diamond. In addition, its non-toxic characteristic is an advantage over the toxic BeO, a potentially serious health hazard concern when processing substrates.

Gallium Phosphide (GaP)

During early development of GaP devices, operational temperatures of up to 450°C were demonstrated with GaP based transistors, and up to 500°C for GaP based thyristors. This makes these devices desirable for long life, high temperature, high frequency applications. A disadvantage is the health concern in processing the highly toxic phosphide radical.

Optoelectronic Product

Three common optoelectronic products are detectors, transmitters, and couplers (transoptors). This section discusses the newer concepts destined for those advanced technologies where at least one of the characteristics such as low-noise, very high speed, high optical resolution, or high sensitivity are paramount to acceptable performance.

Focal Plane Arrays

Mercury/Cadmium/Telluride (HgCdTe) and Gallium Nitrides (GaN, GaAlN) are today's choice for optical focal plane array detectors destined for military and space imaging applications. Indium Phosphide (InP*)* was initially investigated as a good substrate material to grow other high-speed materials upon, and as an InP- *based*, high frequency transistor; however, it was difficult to grow wafers larger than 2 inches. In addition, phosphides are classified as very toxic material. Subsequently, NASA has used HgCdTe on a 3 inch, extremely planer, Sapphire wafer (i.e. imaging 1994 comet-Jupiter collision). GaN and GaAlN on a 6-inch Silicon wafer are under development for UV solar-blind, military applications. Development is also underway using other active materials such as Platinum Silicide for low noise high sensitivity imaging focal arrays, wide band gap II-VI and III-V materials for blue light emitters, Thallium based materials for IR detectors, and, other efforts investigating color discriminating, multispectral, staring arrays that discriminate between targets and background clutter, arrays that provide 3-d imaging, and arrays that have minimal degradation from adverse weather conditions. Commercial use of these imaging technologies is also feasible.

Optoelectronic Couplers

The use of optics/photoconductive materials is not new as a means of signal coupling by the transmission and detection of visible, ultraviolet, or infrared light. Developing technologies, e.g. MCMs are investigating the incorporation of embedded optics. Fiber optics integral to the substrate can efficiently route signals throughout the substrate including optical via paths between multiple layers. Diamond is unsurpassed for optical transmission and adsorption loss and can be used in applications up to 1000°C. The optoelectronic materials previously discussed are also appropriate for transmitting and receiving entities in opto-coupling designs. Optoelectronics can greatly enhance high speed-low signal level performance of integrated circuits by reducing transient times, improving signal-to-noise ratios, and virtually eliminating cross talk

Displays

In a continuing effort to achieve brighter, low power consumption, cost effective displays, a field emission backlight is being developed using a diamond-like carbon that is an electron emitter, which can be deposited onto glass substrates and at room temperatures. It offers a thin profile and extended temperature range. This technology is planned for applications for large, and very bright, commercial outdoor displays, and

is also planned for use as a backlight in a range of liquid crystal displays in aircraft cockpits.

Ferroelectric Liquid Crystal (FLC) Microdisplays

There are three basic types of microdisplays, reflective, transmissive and emissive. The FLC developing technology is a reflective microdisplay using conventional, and reliable, CMOS ICs as blackplanes to control liquid crystal switching. The FLC microdisplays consist of a ferroelectric material sandwiched between a regular CMOS chip and a cover glass. This technology has an advantage of using most of the display surface without loss of area to control circuits. Red, green, and blue LEDs are lit in succession and synchronized to the display drivers to illuminate the display. No color filters or white light source is required. The FLC works as a switchable quarter-wave plate that reflects the LEDs light in two ways; in one state, there is no change in polarization and in the other, there is a 90° rotation in polarization. External polarizing optics is used to change the reflected light into light or dark pixels. Since every pixel produces all three colors, neither triads (subpixels) nor a black matrix is needed as in conventional designs. This results in a sharper image. FLC microdisplays can be designed into either magnified or projected display applications.

ELECTRO-MECHANICAL PRODUCTS

Microelectromechanical Systems (MEMS)

MEMS technology is based on the same fabrication processes and materials being used for integrated microelectronics, but also merges electrical and mechanical micro-components in a single fabrication process. Common processing techniques used in fabricating MEMS include bulk micromachining, wafer-to-wafer bonding, surface micromaching, and high-aspect ratio micromachining. In addition to constructing microelectronic components, MEMS extends the technology to include mechanical components that also have feature sizes at the micron level. MEMS technology combines the advantages of miniaturization, multiple components and microelectronics in the design and construction of integrated electromechanical systems, which have the ability to sense mechanical, thermal, chemical, electrical, and optical occurrences. MEMs can also perform such operations as signaling, moving, positioning, actuating, controlling, regulating, and pumping while providing the advantages of small size, low power, low mass, low-cost and high-functionality. Example applications are: tire pressure sensors, inertial measurement units, distributed sensors both for condition-based maintenance and for structual health and monitoring, distributed unattended sensors both for asset tracking and for environmental, security surveillance, and mass data storage devices.