Microcircuit Packaging

This section describes various packages used in the microcircuit industry. Use this section to support the design and selection of the microcircuit packages.

Packages provide a practical and reliable interconnect pathway for leads and they protect the die from adverse effects of the macro-environment. The package also serves as a heat sink dissipating the thermal energy that is generated during operation away from the microcircuit chip. Packaging, in the military environment, can be divided into two classes: hermetically sealed and plastic encapsulated. Both hermetically sealed and plastic encapsulated packages have several case styles that are configured to satisfy a variety of requirements. There is a predominant trend toward higher density packaging. Plug-in and feed-through terminals are being replaced by surface mount designs that use all four package sides or package bottom pin-outs. The microcircuit chip places demands on the package in terms of:

a. Pad count, pad pitch

b. Die size

c. Power dissipation and thermal management

d. Clock frequency, bandwidth and electrical noise

e. Mechanical reliability

Package Styles

The transition to the surface mount package led to the use of solder pads rather than pins inserted into holes. This was a major advance to more densely packed components on boards and minimized the cost of the boards. Early surface mount packages were Dual-Inline-Packages (DIPs) with their leads cut short and butt attached to the boards, leads that are bent under are called J leads, and leads that are bent out are called gull wing. Packaging quickly evolved to the peripherally leaded package. The term “flat pack” was introduced to describe a new generation of packages designed to be mounted to the surface of the board, with leads on all four sides. In the 1980’s, the term “chip carrier” was introduced. Chip carriers are rectangular or square packages, leaded or leadless, with attach points around the periphery. Early surface mount packages tended to have a much smaller footprint than comparable pin count DIPs or PGAs because of the tighter pitch possible, typically 50mil centers, and using all four sides.
See Figure 1 for the growth of I/O capacity over time for four kinds of packages.

Package styles can be categorized into three classes based on their lead form factor:

a. Dual In-line Package (DIP): Rectangular packages with two rows of leads on two sides of the package, can be through-hole or SMT.

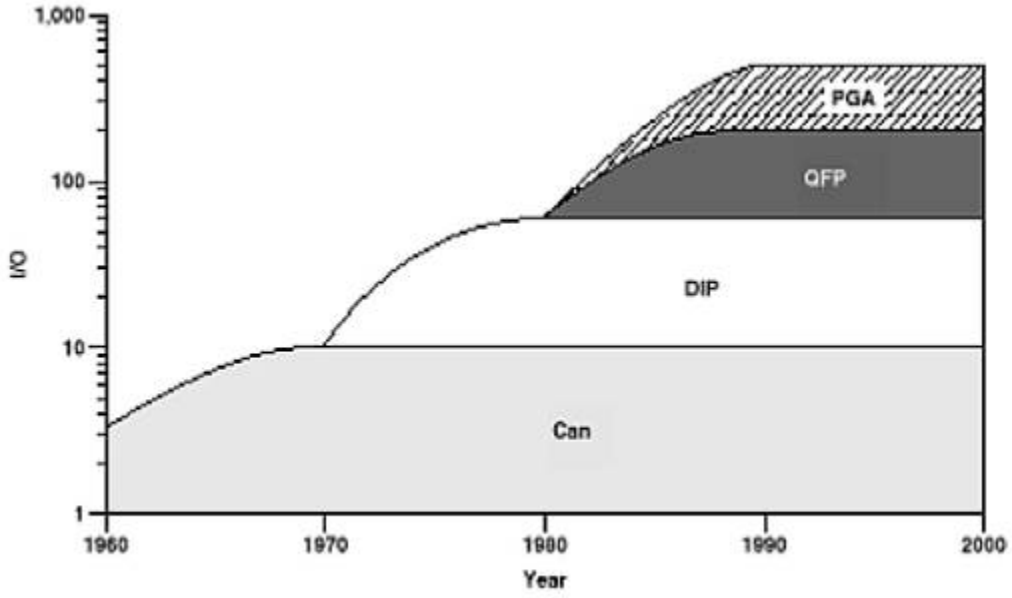

Figure 1. Historical Origin and Evolution of Conventional Packaging
Source: ICE, "Roadmaps of Packaging Technology"

b. Quad Flat Packs (Chip Carriers): Square packages, with leads on all four sides, strictly for SMT.

c. Grid Arrays: Leads/pads/solder balls on an area array. For through hole, called PGA; for SMT, called LGA or BGA.

These package styles are shown in Figure 2. Each package style can be categorized by lead pitch, body size, total number of pins, package thickness, and special enhancements.

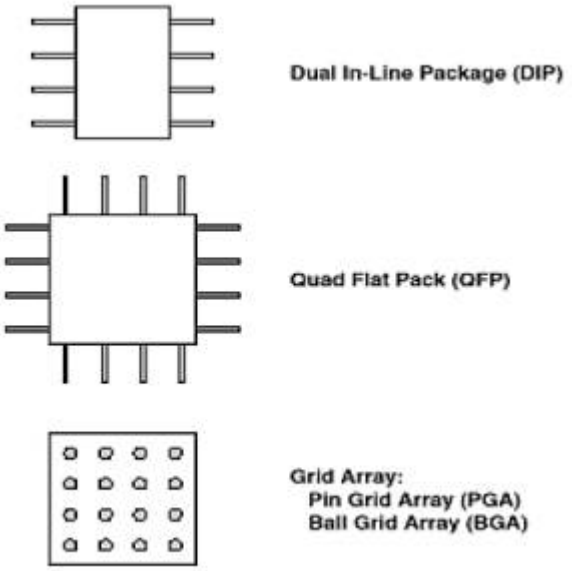

Figure 2. Diagram of Package Sizes

A significant factor of a package is the number of external pins it can support. Each package style has a body size and footprint area that scales with pin count showing the package is pin limited rather than microcircuit size limited. This is illustrated in Figure 3 for each of the three styles.

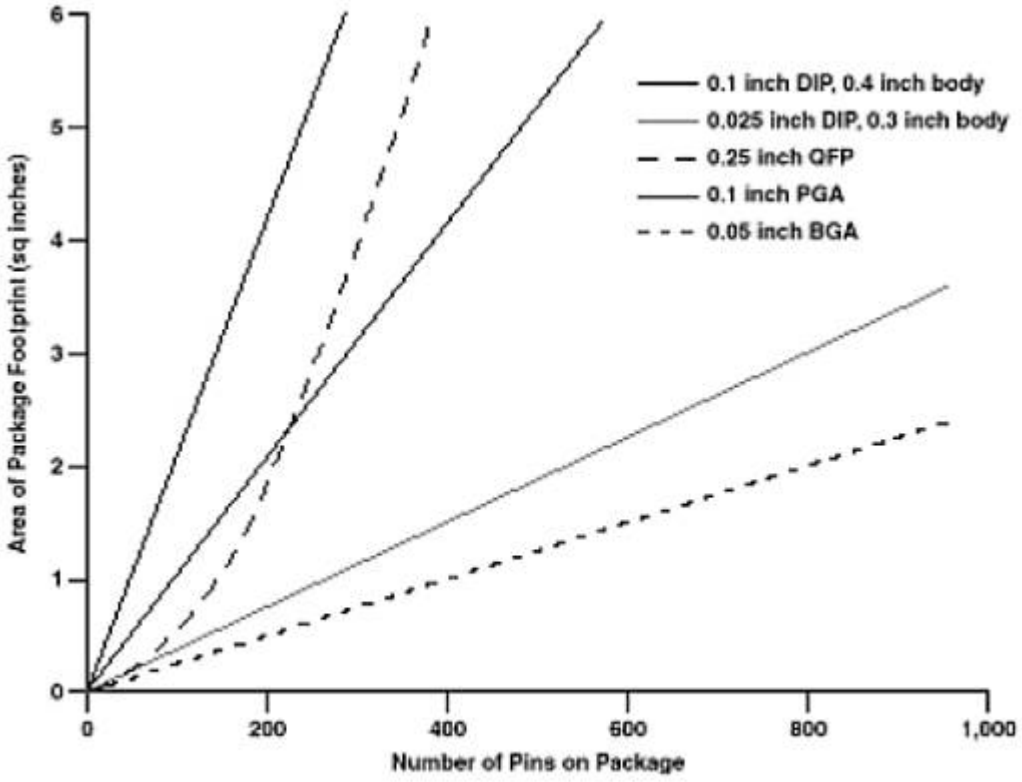

Figure 3. Body Size and Pin Count
Source: ICE, "Roadmaps of Packaging Technology"

For most low pin count microcircuits, a DIP is the preferred package. As pin count increases, the optimum style is a QFP. At about 80 pins, a 50mil center BGA offers a smaller footprint. At about 230 pins, a 100mil center PGA is more optimum over a QFP. For the highest pin counts, the BGA offers the most efficient package footprint

DIP Package Styles

The more commonly used package styles are:

a. Dual-In-Line Package (DIP) created to provide more pins than a metal can while allowing through-hole assembly in conventional circuit boards. The DIP has leads on two sides and dual rows of leads. This style package has evolved to include surface mount versions, but still with leads on only two sides. DIPs are packages used for low pin counts (typically less than 64 pins), usually pin-through-hole, and are made with plastic or ceramic packaging materials.

b. Small Outline Package (SOP). When DIPs are used for surface mount and the pitch is reduced to 25 mils, the package style is often referred to as Small Outline Package (SOP), or Small Outline Integrated Circuit (SOIC). When the leads are bent under in a J lead, rather than straight out as in gull wing, the package style is termed SOJ. Examples are shown in Figure 4. The current driving force on SOPs is to reduce the thickness or profile of the package.

c. Figure 5 illustrates this trend in reduced thickness SOP packaging. As the package gets thinner, the name reflects this, as in Thin SOP, or TSOP, and Very Thin SOP or VTSOP.

Drawing	Nomenclature	Body Width	Lead Type
 8 - 16 Pin	SO = Small Outline	156mil	Gull 50mil Pitch
 8 - 16 Pin	SOM = Medium Outline	220mil	
 16 - 32 Pin	SOL = "Large" Outline SOP = "Small" Outline Package	300mil*	
 16 - 40 Pin	SOJ or SOL-J = "J" - Lead Large Outline	300mil*	J- Lead 50mil
 32 - 56 Pin	VSOP = Very Small Outline Package	300mil	Gull Wing 25mil
 8 - 30 Pin	SSOP = Shrink Small Outline Package	209mil	Gull Wing 25mil
 20 - 56 Pin	TSOP = Thin Small Outline Package	230mil to 550mil Including Leads	Gull Wing Type 1 19.7mil

* Up to 440mils

Figure 4. SOIC Small Outline Microcircuit Packages

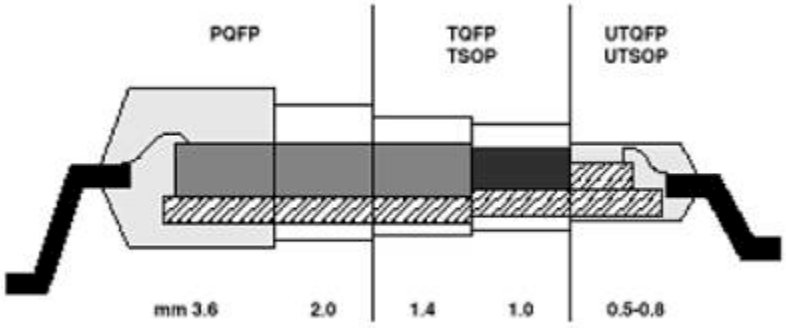

Figure 5. Package-Profile Evolution

Note: The majority of microcircuits are memory and standard logic, which require simple packages, such as SOPs. While SOPs continue to take over from DIPs, at the same time, TQFPs (thin-quad-flat-packs) are beginning to replace some SOPs.

Quad Flat Pack Styles

Quad Flat Pack (QFP) or Chip Carriers have leads on all four sides of the package and are used only for surface mount. When the leads are folded under in a J lead, and plastic molded, they are called PLCC (Plastic Leaded Chip Carriers). A molded plastic QFP is referred to as a Plastic QFP or PQFP. When the QFP is made from cofired ceramic, it is a CQFP. When it is made with a metal base, it is termed MQFP. The MQUAD, which is diagrammed in Figure 6, has a metal clamshell top and bottom with enhanced thermal and electrical performance. The QFP is commonly used for lead counts higher than SOPs since their four-sided design can accommodate more I/Os than SOPs. A 40-mm QFP can be produced with a pitch size as small as 0.5-mm and 304 leads. Because of the complexity of the surface mount assembly process, it is difficult to manufacture QFPs with a pitch less than 0.5-mm and lead counts higher than 304. QFPs are used for low to mid-range lead counts (16 - 304). The growth in QFPs stems from the fact that systems require many chips that dissipate more heat than a SOP can handle. QFPs can take more heat than SOPs but they cannot handle large amounts of heat without artificial cooling such as heat sinks.

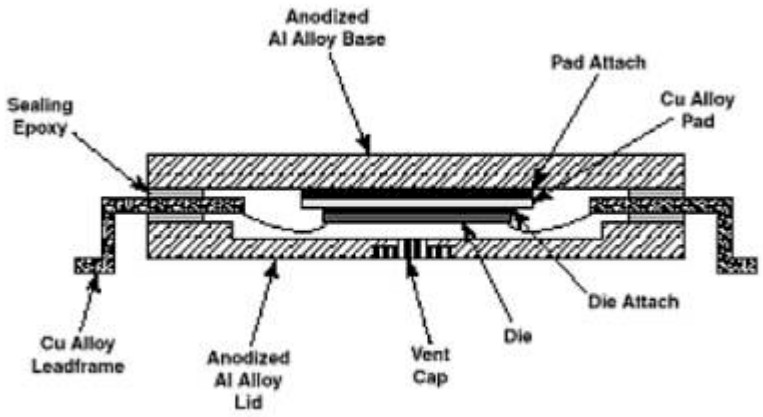

Figure 6. Cavity Down MQUAD® Package

Some common QFPs are:

a. Metric Quad Flat Package (MQFP) is the most common cost-effective, high pin count QFP. Body sizes range from 10 X 10 to 40 X 40 mm with lead counts of 44-304. Many MQFPs are available with metal heat spreaders attached directly to the die or mounted just above the die.

b. Thin Quad Flat Package (TQFP) is available in a variety of body sizes, and lead counts are standard JEDEC formats ranging from 7 X 7 to 28 X 28 mm. Lead counts range from 32 to 256 leads. The TQFP is ideal for assemblies with thickness restrictions such as notebook computers. TQFPs range in size from 20 mm through 28 mm. The TQFP (particularly with fine pitch designs) is fragile and requires careful handling.

c. Very Small Package Array Quad Flat Package (JEDEC PQFP-B) are a scaleable package with good electrical and thermal characteristics. The peripheral lead structure allows for visual inspection. It has a cavity down configuration where the die is attached to a metal base plate providing a direct thermal path to ambient. The die is wire bonded to tiers allowing for more leads in a smaller package. This package uses a liquid crystal polymer frame providing stability up to the melting point of 335°C and is approximately the same size as a comparable PBGA or SBGA. This design offers advantages from a moisture perspective, but being a leaded device, it is somewhat fragile. Examples of QFPs are shown in Figure 7.

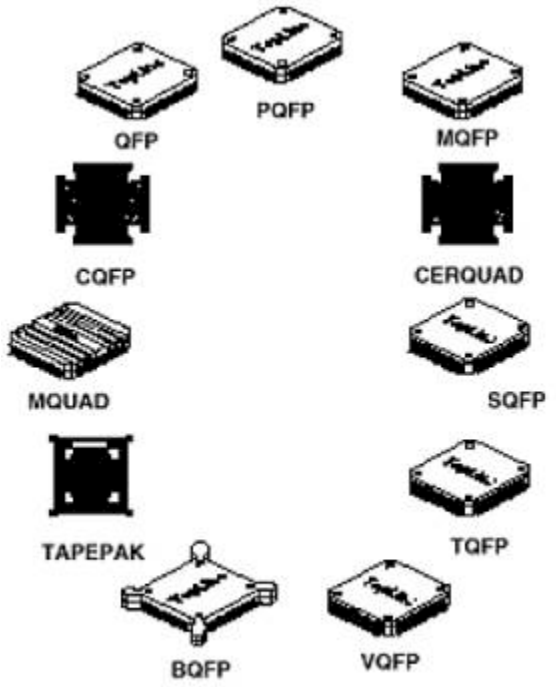

Figure 7. Quad Flat Packs (QFP)

Ball Grid Array Styles

Ball Grid Array (BGA) packages have emerged to provide benefits such as small size, good yields, excellent electrical performance, and high lead count capacity. By spreading the contacts over the bottom of the packaged device, the size of the package is reduced compared to QFPs. The rising numbers of leads per package and lead pitch limitations are the driving forces behind the increasing popularity of BGAs. There are currently nine BGA package outline registrations in JEDEC with over 500 variations. In the past, microcircuit packages have been designed using mechanical-based tools due to the low I/O density of the microcircuits. However, today's IC complexity has brought tighter circuit geometries, higher pad densities, and more layers of metal. Therefore, high-density microcircuit packages and multi-chip modules are becoming more complex in design and are quickly becoming an integral part of system-level performance. The ability to be able to analyze and simulate the package behavior before the package is actually built is critical. In other words, the package design has to be modeled in the same way the complex chips have to be modeled before they are committed to production. There are many varieties of BGA packages but they can be generally categorized as diagrammed in Figure 8 and described as follows:

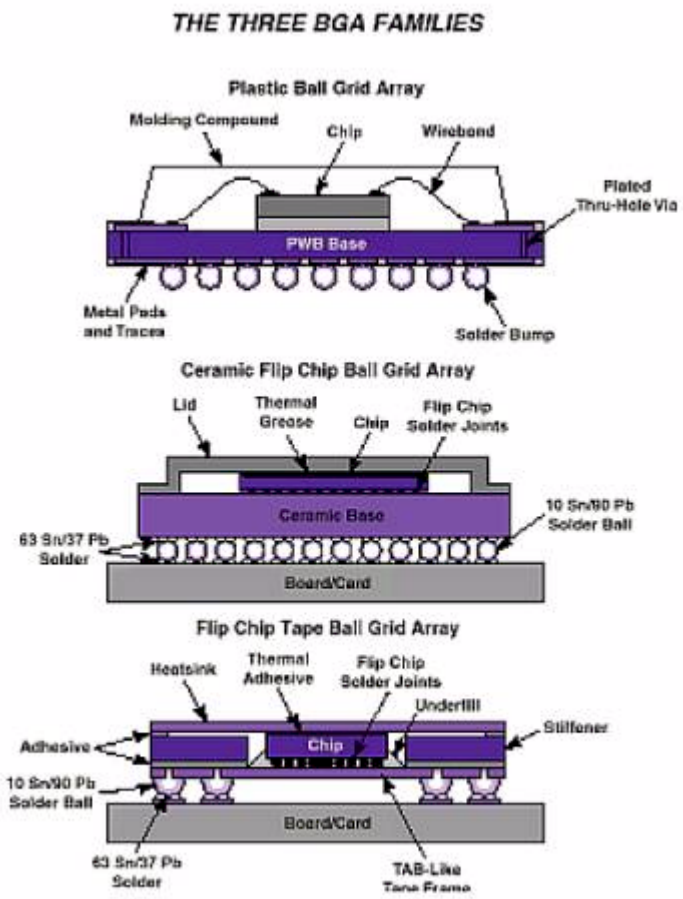

Figure 8. Ball Grid Array Families

a. The Plastic Ball Grid Array (PBGA) and Ceramic Ball Grid Array (CBGA) are the most commonly used. These packages can be manufactured using wire-bonding or flip-chip technology, have enhancements for very low thermal resistance and heatsinks, and have multilayer substrates for enhanced electrical performance. PBGAs are typically used for low power; low density packages with less than 400 contacts, while CBGAs are used for higher performance packages. The PBGA is an ideal replacement for high lead count (100-500) QFPs and TQFPS. It has a die-up configuration with the die wire bonded to a multilayer laminate substrate for distribution of electrical signals to the package solder spheres. The laminate utilizes standard, fine-line multilayer fabrication techniques to provide the signal routing, yet maintain low inductance. The laminate and over-molded plastic constructions provide a close match to the coefficient of thermal expansion (CTE) of the substrate (particularly multilayer FR-4 boards). These packages are moisture sensitive but they are less fragile than QFPs due to the robustness of the solder ball.

b. Tape BGA is popular for high performance microcircuits that require a thinner, lighter weight component. TBGAs are flip-chip packages that are mounted on a polyimide substrate. TBGAs require the use of liquid encapsulates as underfill to reduce the shear stress load on the flip chip interconnections due to the large difference in CTE between the microcircuit and the substrate. Recent tests have demonstrated that TBGAs have advantages over other BGAs in terms of integration levels, defect levels, joint reliability, thermal, and electrical performance.

c. Super Ball Grid Array (BGA) is used when a low-profile device with a high heat tolerance is required. It is ideal for applications requiring 60-600 interconnects, and where a QFP with a heat spreader would be used. This device has a die cavity down configuration where the die is mounted to an integrated copper heat sink and wire bonded to a flexible dielectric substrate with a copper infrastructure providing package rigidity and good heat spreading capabilities. The combination of the flexible dielectric substrate and the eutectic solder joints provide a CTE buffer between the body and the PCB. Compared to the PBGA, the SuperBGA has better heat dissipation, but the cost is higher.

d. Flexible Ball Grid Array (FleXBGA) is used with applications requiring a thin package and reduced ball pitch. The FleXBGA is ideal for applications requiring 100-600 interconnects with a high mounting pad density and a small form factor. This device has a die-up configuration wire bonded to a flexible circuit substrate with fine-line technology for reduced package size. The flexible circuit substrate provides a good CTE match for common laminate substrates and is similar in cost to the PBGA.

e. Fine Pitch Ball Grid Array (FPBGA or mBGA) is a chip scale device designed for applications requiring 30-300 interconnects and an extremely small form factor. Typically, the FPBGA is only 0.4 mm larger than the mounted die. This allows for product miniaturization and reduced signal paths. This package design uses an elastomer pad between the polyimide film (circuitry) and the die that provides mechanical compliance between the package and the PCB. This compliance virtually eliminates solder joint fatigue failures at the PCB level due to CTE mismatch. The FPBGA is significantly smaller than the other BGAs of comparable interconnects. Final package size is die dependent. The decreasing cost of the FPBGA is making it a viable option for replacing lead frame packages.

Note: The package of choice for microprocessors and complex ASICs is the BGA. BGAs can handle a high number of leads on a footprint smaller than a QFP, and if heatsinks are provided, they can also handle high amounts of heat. BGAs are in virtually every computer, workstation, and server to house chips with high lead counts.

Package Standard

The Joint Electronics Devices Engineering Council (JEDEC) JC-11 Committee on Mechanical Standardization creates outlines in Publication 95 (JEDEC Registered and Standard Outlines for Semiconductor Devices) for Standard Microcircuit packages. When designing-in-packages, emphasis should be on using packages registered in JEDEC 95.