Microcircuit Material Issues

Copper

Copper is beginning to be used because it allows the microcircuits to go at higher speeds. The advantage copper has over aluminum is that copper has less resistance and therefore allows electrons to flow faster. This reduces the chip interconnect delays and results in increased speed for semiconductor devices. The use of copper also reduces power consumption. Copper may prove to be a necessity as transistor sizes go to 0.18-micron and beyond. As the circuit size is decreased, the signal-current densities increase and more heat is generated. Copper can support much higher current densities than aluminum because it has a higher melting point. In addition, copper is more reliable than aluminum under the same current densities. Another problem that arises with smaller geometries is crosstalk (the leakage of electrons). Because copper is a better conductor than aluminum it is less likely to leak electrons. Using better dielectric materials with lower dielectric constant (k) values can also alleviate crosstalk. They're some issues with copper that need consideration:

a. Copper is difficult to etch. Manufacturers have to change their deposition and etch steps. The industry is adapting the Damascene process in which the interconnect lines and vias are etched to remove the dielectric materials instead of the metal, whereas with aluminum the metal is etched. This switch to dielectric etch from metal etch has created new requirements for etching tools and technology.

b. The need to deposit the damascene barrier and seed layers before copper deposition is a problem. The purpose of the barrier layer is to prevent the copper from diffusing into the dielectric material and destroying the transistors. The Damascene process starts with a layer of dielectric material that is etched by photolithography to produce the circuit pattern. A barrier layer (typically a few hundred angstroms of refractory titanium or tungsten-nitride) is applied to the etched pattern. On the barrier layer, a very thin seed layer is deposited by physical-vapor deposition to serve as a "primer" on which the copper is laid. Since the few-hundred-angstrom barrier layer is deposited in the circuitry prior to the copper, the barrier layer reduces the height and width of the copper trace; therefore reducing the resulting overall thickness of the copper interconnect. The thinner the copper interconnect is, the higher the resistivity will be and at very fine geometries the barrier layer can have a dramatic impact on the speed of the circuitry.

c. Depositing microscopic copper interconnects on a microcircuit is very difficult. The problem lies with the high aspect ratios presented by the 0.25 micron and below vias and holes that can have depths as great as 1.0 micron. It is hard to completely fill in the etched pattern in the dielectric and this can result in voids and small cracks in the copper leading to opens in the microcircuit.

d. Current processes for copper deposition are chemical-vapor-deposition (CVD) and electrochemical plating; they both have problems with the very fine pitch geometry.

e. Copper does not mix well with current dielectric materials used for aluminum. Copper can diffuse quickly through the insulating oxides (dielectrics) and into the silicon, destroying the transistors (hence, the use of the barrier layer mentioned above).

Signal Propagation

Speeding up signal propagation through the microcircuit can be accomplished by using a dielectric material with a low k. The lower k will speed up the signal by decreasing the charge buildup between the conductive lines. Some issues with new dielectrics that need consideration are detailed below:

a. The shift to 0.18-μm and smaller process geometries and copper interconnects places new requirements on dielectric materials used in fabrication. With geometries over 0.5μm, silicon dioxide, with a k of about 4, was used successfully to isolate layers of metals. As linewidths have gotten smaller, the use of silicon dioxide is no longer feasible because its relatively high k value creates excessive charge build-up on the metal lines and slows the signal propagation.

b. The capacitance increases as k increases, and the capacitance increases as the linewidths get smaller. It is important to use low-k dielectrics with small geometry microcircuits. Wire delay increases as a percentage of total delay in the smaller geometries. Manufacturers are using dielectric materials with constants of between 3.0 and 4.0 for their 0.18μm processes. To go to 0.15μm and below, dielectric constants will need to be limited to 3.0 or less.

c. An ideal low-k material is one that offers a low dielectric constant and has similar properties as silicon-dioxide, such as low leakage, low thermal coefficient of expansion (<10 ppm/C), high dielectric break-down voltage (2-3 MV/cm), low film stress, low water absorption, high cracking resistance, and adhesion to other materials.

d. Another critical factor is the ability to integrate the low-k materials easily into the manufacturing process. Low-k materials have been difficult and expensive to integrate into production lines and are poor thermal conductors.

e. Making the material porous can lower the dielectric constant of organic polymers. For example, a polymer with a k value of 2.65 can be modified to have a k value of just about 2.0 by putting 20% porosity in the polymer.