Microcircuit Electrical Issues

Distortion

The frequency at which transmitted power has dropped to 50 percent of the injected power is called the "3 dB" point and is used to define the bandwidth of the interconnect. This is the highest sine wave frequency at which the interconnect can be used. For some applications, more than 3dB may be acceptable, in other applications, less than 3dB will be acceptable. 3dB drop in power corresponds to a drop of 30% in voltage amplitude. This is the noise margin in most device families. If a signal were to drop by 30% in amplitude, it would most likely not meet specifications, so the criterion of 3dB is reasonable for digital microcircuits. Distortions in the interconnect decrease the bandwidth of transmitted signals and increase rise-times of transmitted signals. Distortion of the pristine waveforms coming from the junctions is caused by on-chip metallization, packaging, and interconnects which creates parasitic capacitance, inductance and resistance. This distortion limits the rise-time of signals that propagate in the interconnect environment, increasing the minimum possible clock period. Distortion from packages and interconnects can be so severe as to cause false triggering. Rise-time degradation and clock skew can slow the operating clock frequency below the specified value. As the clock frequency and interconnect density increase, it becomes harder for the interconnect system to maintain the signal integrity within acceptable levels.

Rise-Time Degradation

A decrease in the bandwidth of a signal causes an increase in the leading edge rise-time. This rise-time degradation will introduce a delay until the voltage level reaches the triggering threshold, which increases the effective wiring delay.

Bandwidth

The clock frequency does not determine the bandwidth, the rise-time of the signal does. In digital microcircuits, there is a connection between rise-time and clock frequency. As the rise-time drops, this is an indication that the microcircuit is capable of switching faster, and the clock frequency usually increases. Depending on the type of digital system there are between 5 and 10 rise-times per clock period.

Noise Level

An acceptable noise level is a major concern for interconnect designs. The interconnect transports the signal to and from each node with an acceptable level of distortion, and also transports the DC power and ground to all the microcircuits

with an acceptable noise level. The criterion of what is acceptable noise comes from the noise margin of the microcircuit family. The noise margin is the difference between the worst case output voltage and the minimum acceptable input voltage. There are three primary sources of noise: signal integrity down a single trace, crosstalk from adjacent lines, and switching noise from the power and ground distribution.

Ringing

Ringing can become a significant problem at higher bandwidths. It can be eliminated by placing a damping resistor at the source. Another suppression technique is to use ground planes in packages to minimize leadframe inductances and to control the impedance of interconnect traces. In addition, series damping resistors may be added to the circuits in such a way as to avoid an added hit from RC delays. Ringing and reflection noise increases in magnitude as the bandwidth of the signal increases and the rise-time decreases; therefore most high-speed microcircuits have the option of using reduced slew rate output buffers so the packaging does not seriously degrade the signal integrity. A longer spatial extent will make the signal less sensitive to interconnect imperfections.

Crosstalk Noise

Crosstalk noise is due to capacitive and inductive coupling between two traces. When two traces run parallel to each other, there is the possibility of coupling voltage from one to the other. The line that is generating the noise is termed the active line or aggressor and the trace on which the noise appears is termed the quiet line or victim line. The magnitude of the coupled noise, V_{quiet}/V_{active}, depends on:

a. The pitch between the traces

b. The characteristic impedance of the traces

c. The dielectric constant of the material surrounding the traces

d. The fraction of the length of the quiet line over which the traces are adjacent

The noise allocated for near-end crosstalk is typically about 3%. A lower dielectric constant for the same pitch will decrease the crosstalk. With FR-4, a 50-Ohm microstrip has a linewidth about twice the dielectric thickness. To keep the crosstalk below 3%, the spacing should be at least 4x the dielectric thickness. In asymmetric strip line, the lower dielectric thickness is about equal to the linewidth for 50 Ohms. To keep the crosstalk to less than 3% requires spacing about 2x the lower dielectric thickness.

Simultaneous Switching Noise

Simultaneous switching noise (also called, ground bounce, or delta I noise) causes a problem in packaging high-performance CMOS microcircuits. This is due to the inductance of the power and ground distribution to the chips and the transient current from output buffers. All of the inductance of the power and ground distribution traces, from the chip to the nearest decoupling capacitor, must be included. In simultaneous switching, it is the inductance associated with the ground connection of the chip bonding, such as the wirebond and leadframe, that plays the most critical role. Usually, a number of buffer gates are tied to the same ground rail. In leading edge CMOS microcircuits, the number of gates switching simultaneously is increasing and the switching transition time is decreasing. Both of these effects are increasing the impact of simultaneous switching noise. Minimizing this problem requires solutions that address:

a. The chip drivers: All high-speed gate arrays currently have available the option of selecting a slower output buffer slew rate to decrease the bandwidth of the output signal.

b. The number of outputs sharing the same ground line: Though there is a minimum number of power and ground pads that must be used on a chip, the designer has the option of adding more. The trend is to appropriate all unused, available pads for extra power and ground. This approach has the double benefit of reducing the inductance associated with the power and ground connections and decoupling sensitive gates from their neighbors. For 50MHz ASICs, minimum guidelines call for one ground for every 16 gates. This number is rapidly approaching one for every four output buffers in 200MHz ASICs. This is another driving force causing increases in the off-chip pin count.

c. The inductance of the chip attach: It is the inductance of the ground path section of the circuit that influences the switching noise. The inductance of the package leadframe and chip bonding can be decreased. Ground planes in the Packages are the first step to decrease leadframe inductance. Chip bonding inductance can be decreased by designing shorter wirebond lengths or by using flip chip. This is a strong driver for the use of flip chip die attaches. Decoupling capacitors can be attached as close as possible to the chip, either on the multilayer package or directly under the chip package.

d. The output capacitance that is driven: The capacitance that must be driven by each buffer can be decreased as a spin-off of higher packaging efficiencies driven by higher clock frequencies.

Ground Leads

Shortening ground leads by bringing them to the center of long packages, and bringing high current carrying signal leads in proximity to the ground leads can dramatically reduce switching noise. This change reduced the effective inductance of ground leads by a factor of 5 between the old and the new pinouts.
High speed problems.
There are four design guidelines that should minimize 80% of high-speed problems:

a. Keep the interconnects as short as possible. This will minimize delay times, clock skew and signal integrity problems.

b. Use controlled impedance interconnects, at roughly 50 Ohms characteristic impedance. This minimizes reflection noise and keeps EMI low.

c. Keep adjacent traces far enough apart so that crosstalk is below the specification, typically 3% coupling or less.

d. Keep the impedance of the power and ground distribution low, using planes where possible. Keep all leads as short as possible to reduce switching noise.

Timing Errors

Timing errors need to be avoided when designing high-speed applications. Excessive propagation delay or race conditions are the cause. Excessive propagation delay is when the propagation delay of a circuit is longer than the clock period. A race condition occurs when a gate does not have all its inputs when needed, compared to the clock, because other gates were switched either too late or too early due to clock skew. Being able to predict and control clock skew to less than one gate delay is of great importance. Within one clock cycle, the number of gates that must switch sequentially is called the logic depth, N logic depth. This is typically 10 to 20. The length of time it takes for the signal to propagate through the longest path will establish the shortest clock period. In a system with a 50MHz-clock frequency, typically 5 to 10 percent of the nets are critical in that their total propagation delay may approach the clock period. In very high-speed systems with clock frequencies above 100MHz, 20 to 50 percent of the nets could be critical. The propagation delay of a net will depend on the delays associated with each part of the net: the gate delays, the on-chip interconnect delays, the output buffer delays, the delays associated with the packages, and the wiring delays between packages.

Interconnects

Interconnects at low frequency are effectively transparent and no special design rules are required; however, interconnects at high frequency do need special care. Described below are three effects that may arise and prevent an application from working.

a. Exceeding the timing margin from race-conditions between the data stream and effects that may arise that will prevent the design from working.

b. Exceeding the noise margin from:

1) waveform distortion and decreased signal integrity

2) crosstalk between adjacent traces

3) noise in the power and ground distribution system, such as ground bounce and simultaneous switching noise or IR drop

c. Exceeding the EMI margin by common or differential mode radiation