MCM & Hybrid Design and Material

This section is to be used as guidance to support the design and selection of MCMs and/or Hybrids.

MCMs and Hybrids are similar in many aspects of manufacturing and usage; however, there are differences in typical designs. Hybrids are usually designed to produce a circuit function unavailable in a single monolithic microcircuit package, and consist of individual active and passive chips (bare-die) combined with discrete devices. MCMs are usually designed to provide a system function(s) in applications with very limited real estate, and consist solely of active and passive chips (bare-die). Hybrid substrates traditionally are thick-film based, while MCMs may be thick film, thin film, or lament. A product consisting of a diverse variety of bare-die is an MCM, but might also be considered a Hybrid. However, a product containing both chips and discretes can only be classified as a Hybrid.

General Rework and Repair

a. Touch-up of package sealing surface plating on delidded packages should not be permitted.

b. For seam welding, the minimum distance between the glass to metal seals and the package sealing surface should be at least .040 inch (1.02 mm) after final seal, to prevent damage to lead seals by welding adjacent to them.

c. Replacement elements should not be bonded onto the chip element that they are to replace.

d. Rework of a wafer (i.e., the strip and redeposition of a layer in order to correct a nonconformance to a specification limit) should not be allowed. Additional etch to correct a nonconformance to a specification limit, photoresist strip and recoat, or processing to continue or finish incomplete processing, should not be considered rework.

Wire Rebonding.

a. Wire rebonding of elements other than substrates, thick film elements, capacitors, and package posts should be permitted with the following limitations:

1. No scratched, voided, or discontinuous paths or conductor patterns on an element should be repaired by bridging with or addition of bonding wire or ribbon.

2. All rebonds should be placed on at least 50 percent undisturbed metal (excluding probe marks that do not expose underlying oxide). No more than one rebond attempt at any design bond location should be permitted. No rebonds should touch an area of exposed oxide caused by lifted or blistered metal. Bond-offs required to clear the bonder after an unsuccessful bond attempt need not be visible, should not be cause for reject, and should not be counted as a rebond.

b. Wire rebonding on substrates and package posts should be permitted with the following limitations:

1. Scratched, open, or discontinuous substrate metallization paths or conductor pattern on a substrate, not caused by poor adhesion, may be repaired by bridging with or by addition of bonded conductors having current carrying capacity at least 3.5 times the maximum calculated operating load current for the conductor or 3.5 times the current capacity of the wire bond connection terminating on the damaged conductor path. The quantity of repairs should be limited to one for each one-half square inch or fraction thereof of substrate area. This repair is not applicable to thick film elements, capacitors, or package posts.

2. No rebonds should be made over intended bonding areas in which the top layer metallization has lifted, peeled, or has been damaged such that underlying metallization or substrate is exposed at the immediate bond site.

Compound Bonding

Compound bonding should be permitted only as follows:

a. When required for design, rework, or repair, gold compound bonds should be limited to one bond over the original bond, wire, or ribbon.

b. Only monometallic compound bonds of the same size wire or ribbon should be permitted (i.e., the original bond wire and that used for compound bonding should be the same material).

c. For rework or repair, the maximum number of compound bonds should not exceed 10 percent of the total number of wires.

d For rework or repair, a corrective action system should be utilized in order to reduce the number of compound bonds.

e For rework or repair, all compound bonds should be 100 percent nondestructive pull tested in accordance with MIL-STD-883, Method 2023.

f. A compound bond should not be used to connect two wires.

g. All compound bonds should meet the visual criteria in MIL-STD-883, Method 2017.

Element Replacement

Element replacement should be permitted with the following limitations:

a. Any polymer-attached element may be replaced two times at a given location on any device.

b. Any element attached with polymer to metal, other than substrate metallization (e.g., pedestals, ribs, carriers, etc.), may be replaced four times at a given location.

c. The number of polymer attached tuning element replacements should be defined in the manufacturers' baseline documentation.

Use of Polymers

The use of polymers to effect, improve, or repair any package seal should not be permitted.

Seal Rework

It is permissible to perform seal rework without delidding on devices that fail fine leak testing one time, only if tracer gas is included during the original sealing operation and under all of the following conditions:

a. Fine leak testing, without pressurization (bomb), should be performed immediately after sealing, before any other test.

b. Devices should be stored in a nitrogen environment for a maximum of 4 hours between initial seal and reseal, without replacing the cover.

c. Devices should be submitted to a predetermined vacuum bake before reseal.

d. Solder sealed packages may not be reworked in accordance with this procedure.

It is permissible to rework other seals (e.g., feedthroughs, connectors, seal plugs, windows, etc.) at metal-to-metal interfaces on unlidded devices.

Delidding and Relidding

Devices may be delidded and relidded for rework or repair provided the delid-relid procedures, controls, and resulting data are baselined. Delid-relid history (e.g., traceability by lot number or serial numbers) should be maintained by the device manufacturer.

Only seam sealed, overlapping pulse welded, or laser welded packages designed for delid-relid may be delidded-relidded.

Package Construction and Sealing

Devices should be hermetically sealed in glass, metal, or ceramic (or combinations of these) packages. The following provisions apply to package construction and sealing:

a. No adhesive or polymeric materials will be used for package lid, or feedthrough, attach (or seal) or rework/repair.

b. Polymer impregnations or secondary seal (backfill, coating, or other uses or organic or polymeric materials to effect, improve, or rework/repair the seal) on the device package should not be permitted.

c. Flux should not be used in the final sealing process.

d. In the case of final lid seal using a welding process, sufficient distance should be maintained between the lid seal and any glass-to-metal seal, to preclude damage or degradation of the glass-to-metal seal.

e. Package materials should be selected such, that thermal expansion rate mismatches between different materials do not compromise package integrity or hermetically during applicable temperature excursions.

Cure Temperature

The cure temperature of polymeric materials should not be exceeded after completion of final seal. Polymeric materials should meet the requirements of MIL-STD-883, Method 5011.

External Metal Surfaces

External metal surfaces, other than seal weld areas, should meet the applicable corrosion resistance requirements, or should be plated to do so.

Integrity of Externals

External parts, elements, or coatings, including markings, should be non-nutrient to fungus and should not blister, crack, flow, or exhibit defects that adversely

affect storage, operation, or environmental capabilities of the device under the specified test and operating conditions.

Internal Thin Film Conductors

Internal thin film conductors on elements (metallization stripes, contact areas, bonding interfaces, etc.) and internal wires (wires, ribbons, etc.) should be designed such that no properly fabricated conductor should experience current in excess of the maximum value calculated by the manufacturer to preclude damage or degradation to the conductors, except by design (e.g., internal fuses). The following conditions should be considered when calculating the maximum current:

a. Calculate the current density at the point of maximum current density (i.e., greatest current per unit cross section) for the specified device type.

b. Use a current value equal to the maximum continuous current (at full fanout for digitals or at maximum load for linears) or equal to the simple time-averaged current, obtained at maximum rated frequency and duty cycle with maximum load, whichever results in the greater current value at the point of maximum current density. This current value should be determined at the maximum recommended supply voltage and with the current assumed uniform over the entire conductor cross-sectional area.

c. Use the minimum allowed metal thickness in accordance with manufacturing specifications and controls, including appropriate allowance for thinning experienced in the metallization step (via). The thinning factor over a metallization step is not required unless the point of maximum current density is located at the step.

d. Use the minimum allowable actual conductor widths (not mask widths) including appropriate allowance for narrowing or undercutting experienced in metal etching.

e. Do not include areas of barrier metals and nonconducting material in the calculation of conductor cross-section.

Finish

Tin should be prohibited as a final finish and as an undercoat. The use of tin-lead finish is acceptable if the lead content is a minimum of 2 percent by weight.

Leads

Lead finish thickness measurements should be taken halfway between the seating plane and the tip of the lead. The finish system on all-external leads or terminals should conform to one of the following:

a. Hot solder dip. The hot solder dip will be homogeneous with a minimum thickness of 60 microinches (1.52 μm) for round leads and, for other shapes, a minimum thickness at the crest of the major flats of 200 microinches (5.08 μm) solder (SN60 or SN63). For leadless chip carrier devices, the solder will cover a minimum of 95 percent of the metallized side castellation or notch and metallized areas above and below the notch (except the index feature if not connected to the castellation). Terminal area intended for device mounting will be completely covered. The hot solder dip on leads is applicable to either 1 or 2 below:

1. Over a finish in accordance with entry c or d below. The solder will extend within 0.030 inch (0.76 mm) of the lead or package interface, or beyond the effective seating plane for packages with standoffs.

2. Over the basis metal or other finishes. When applied over the basis metal, or over underplate or finishes other than as specified in entry c or d, solder will cover the entire lead to the glass seal or point of emergence of the lead or metallized contact through the package wall.

b. Tin-lead plate. Tin-lead plate will have in the plated deposit 2 percent to 50 percent by weight lead (balance nominally tin) co-deposited. As plated, tin-lead will be a minimum of 300 microinches thick and will contain no more than 0.05 percent by weight co-deposited organic material (measured as elemental carbon). Tin-lead plating may be fused by heating above its liquidus temperature. Fused tin-lead will be a minimum of 200 microinches thick. Tin-lead plate is applicable:

1. Over a finish in accordance with entry c below, or

2. Over the basis metal.

c. Nickel plate or undercoating. Electroplated nickel or electroless nickel phosphorous nickel undercoating or finishes will be 50 to 350 microinches (1.27 μm to 8.89 μm) thick measured on major flats or diameters. Electroless nickel will not be used as the undercoating on flexible or semiflexible leads and will be permitted only on rigid leads or package elements other than leads (see MIL-STD-883 Method 2004 for definitions of flexible and semiflexible leads).

d. Gold plate. Gold plating will be a minimum of 99.78 percent gold, and only cobalt will be used as the hardener. Gold plating will be a minimum of 50 microinches (1.27 μm) and a maximum of 225 microinches (5.72 μm) thick. Gold

plating will be permitted only over nickel plate or undercoating in accordance with entry c above.

Design Analyses

Thermal design analysis should be performed. As a minimum, it should establish that functional device elements are operating within their design temperature ratings when the device is operated at the specified maximum operating case temperature. Finite element analysis is an acceptable thermal design analysis technique. All active and passive elements should be derated.

Worst case circuit design analysis should be performed and include the following evaluations as a minimum (applicable to the design):

a. Electrical element stress over the specified operating temperature range will be within the specified derating criteria under worst case temperature conditions.

b. Evaluated to meet the Group A CI test limits at worse case operating temperature conditions, as applicable.