Discrete Semiconductors Failure Mechanisms and Anomalies

This section describes common failure mechanisms and anomalies for Discrete Semiconductors. Use this section to select and design Discrete Semiconductors. Table 1 describes common failure mechanisms and tests/monitors for silicon Discrete Semiconductors.

Table 1. Common Failure Mechanisms and Tests/Monitors for Silicon Discrete Semiconductors

Failure Mechanism	**Test/Monitor**	**Comment**
1. Particles	PIND test/Package sealing process monitor	Failure in cavity package usually larger than T0-5
2. Chemical contamination	High Temperature Reverse Bias (HTRB)	Accelerated infant mortality failures due to ion contamination on die
3. Poor or defective construction and/or mechanical stress	Thermal Impedance, Thermal Resistance, Surge, Safe Operating Area (SOA)	Commercial parts and/or poor quality of material and/or poor assembly process control
4. Moisture	Highly Accelerated Stress Test (HAST)	Small outline plastic packages - SMDs
5. Poor metallurgical bond	Thermal Impedance test	Commercial and pressure contact parts
6. Epoxy moisture sensitivity level	Pre-conditioning /Package classification	Small thin plastic packages - SMDs

GaAs Discrete Semiconductors

GaAs failure mechanisms are controlled for channel temperatures below 150°C. Potential solutions to GaAs failure mechanisms are summarized in Table 2. There are at least two mechanisms which determine the ultimate life of the GaAs FETs: ohmic contact degradation and channel degradation. These mechanisms come into play only at very high-temperatures in high-power applications.

Table 2. Common GaAs FET Failure Mechanisms

Mechanisms	**Description**	**Solution**
Gate Metal Sinking	Gate metal reacts with GaAs moving interface into channel Degradation of Schottky junction.	Optimize metallization process using non-reactive materials, control of thickness.

Electromigration	Self-diffusion of drain or gate metal at high current density and temperature.	Gold gate metal, Control current density, Coat with nitride.
Surface Degradation	Oxidation of GaAs releases free Arsenic; Reaction with SiO_2 causes erosion; Mobile ions in passivation.	Plasma Enhanced Chemical Vapor Deposited silicon nitride passivation.
Ohmic Contact Degradation	Out-diffusion of Ga, in-diffusion of Au.	Barrier layers between contact and top Au.
Instantaneous Burnout (incl. ESD)	Breakdown and melting at drain contact.	n+ ledge at drain contact.
	Power dissipation causes Buffer to become intrinsic.	Control thermal resistance.
Long-term Burnout	Reaction of GaAs with surface oxide releasing free Arsenic.	PCVD nitride passivation.
Intermetallic Phase Formation	Kirkendall voiding due to Au-Al interdiffusion aided by electromigration.	Use of All Au system: Separate Au and Al.
Channel Degradation	Diffusion of dopant from channel; diffusion of defects or traps into channel.	No known solution.

The failure mechanisms in Table 2 are described in more detail below.

a. Gate Metal Sinking refers to a mechanism, which the channel depth decreases when the gate metal diffuses down into the GaAs, effectively moving the Schottky barrier deeper into the part. The effect is accompanied by a decrease in I_{dss}, g_m, and pinch-off voltage. The gate sinking mechanism occurs when the gate metal diffuses into the GaAs. Defects in the FETs barrier can lead to local diffusion of gold through the barrier, resulting in premature failure due to localized gate sinking. This usually occurs at the edges of gates where shadowing has resulted in thinner barrier metal deposition.

b. Electromigration is the movement of metal atoms in a conductor carrying a high current caused by momentum exchange between moving electrons and the atoms. This is an important mechanism in high-frequency power transistors where high current densities and high temperature can occur simultaneously. Electromigration results in voids forming in the metal and in the accumulation of metal atoms. When the voids increase enough, they may sever a metal run causing part failure. Likewise, when the metal accumulation becomes large enough in the lateral or vertical (under metal air bridges) direction, they can cause shorting between conductors. This effect varies significantly for different metals; for example, the lighter metals such as aluminum are more

susceptible. The rate of electromigration varies as approximately the square of the current density and has an activation energy, which varies from 0.5 eV to greater than 1 eV, depending on the metal and its structure. Electromigration was an early failure mechanism in GaAs FETs. Electromigration in the drain and source metallization have lead to failures when metal accumulates, causing shorting to air bridges or other adjacent structures. Covering the metal with Silicon Dioxide (SiO2) or silicon nitride (Si3N4) will retard Electromigration.

c. GaAs FETs and HEMTs are susceptible to several different forms of surface degradation, which affect their ultimate life. Described are failure modes:

> 1. Unpassivated parts are subject to surface oxidation which releases free arsenic. The result is a reduction in breakdown voltage, and an increase in low voltage gate current. Because of the breakdown voltage reduction, the power output is decreased and eventually catastrophic failures occur due to gate-drain breakdown.
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> 2. Parts passivated with SiO_2 experience erosion of the GaAs surface, due to an interaction of the GaAs with the SiO_2. This results in a narrowing of the channel and an increase in the source and drain resistance. Mobile ion contamination of the oxide or nitride passivation can result in instability. The effect is an increase in source resistance, due to an increase in the surface depletion layer, which narrows the channel depth. The original performance can be recovered by a 175°C/24-hour bake. Passivation of the surface above the active layer is necessary to prevent instabilities.SiO_2 is not an adequate passivation and sputtered silicon nitride may not be suitable because of mobile ion content.

d. The ohmic contacts to GaAs parts can increase in resistance with time at elevated temperature, eventually leading to wear-out failure. The most common metal system for the contacts is Gold Germanium/Nickel (AuGe/Ni). Typically, their activation energy is 1.4 to 1.8 eV with a Mean-Time-Between-Failure (MTBF) of greater than 10^8 hours at 100°C. This may provide adequate contact life at a operating temperature below 100° C, but rapid degradation can result at temperatures above 150°C. The mechanism involved with this degradation is the continued alloying and intermixing of the

contact metals. In particular, nonstochiometric regions are formed when Ga diffuses through the AuGe into the Au layer, while Au diffuses inward forming high resistive alloys, which causes the contact resistance to increase.

e. Source-drain burnout is a common failure mode of GaAs FETs, accounting for 30 to 50% failures. This catastrophic failure mode results in substantial melting in the active region due to thermal runaway. There are two types of burnout of concern: instantaneous and long term, each caused by different mechanisms. Instantaneous burnout, including ESD failures, will occur when the applied source-drain voltage exceeds the breakdown voltage. Long-term burnout occurs during DC aging, resulting in catastrophic failure after the device has been stressed for some time. This burnout is associated with changes at the surface of the device near the drain contact. Before breakdown, light emission is observed near the drain contact of n+ ledge, associated with microplasmas or localized breakdown sites.

f. Many FETs use Al gate metallization and AuGeNi ohmic contacts. Gold metallization is used for the wire bonding pads because it is compatible with the ohmic contact materials and the gold wires used to package the devices. Consequently, a transition is required between the Al gate metal and the Au pad metal. Early devices had an Au-Al contact between the gate and pad. When stressed at elevated temperatures, Au-Al intermetallic phase formation occurred and device failure resulted due to Kirkendall voiding. This same “purple plague” mechanism has been a traditional failure mechanism in silicon devices in which Au wires are used to connect to Al metallization. Later GaAs FETs employed a barrier layer between the Au and Al to prevent interdiffusion. Although this barrier has been effective in reducing the effect, failures were still observed at high temperatures. Gold apparently migrated along the surface to interact with the Al gate fingers.

High Electron Mobility Transistors (HEMTs) are a new version of a FET, which are of interest at very high frequencies and in applications where very high performance is required. They are a heterostructure consisting of a pure GaAs buffer layer overlaid by a doped AlGaAs layer. The lateral geometry of the HEMT is very similar to that of a GaAs FET with similar gate and contact structures.