# Discrete Semiconductors Design and Material

This section describes issues of importance to the performance of a Discrete Semiconductor. Use this section to support the design and selection of Discrete Semiconductors.

a. Unless it is part of the original design, the external surface of package, header, or flange should be finished and not have any depression or cavity. External parts, elements, or coatings should not blister, crack, (excluding glass meniscus), outgas, soften, flow, or exhibit defects that adversely affect storage, operation, or environmental capabilities of semiconductor devices. The use of silicone or organic material inside the packages should be approved. Desiccants should not be used. Polymer impregnation (such as backfill) of the packages should not be permitted.

b. Pure glass should not be used for die mounting. Die attachment procedures are critical, because, in addition to its relation to mechanical integrity, die attachment is the first step in establishing a good thermal path to remove heat generated in the part and it determines the effectiveness of the ground plane. It is recommended for GaAs-based parts that Au/Sn eutectic die attachments are used for discrete FETs. Equal success can be accomplished with conductive epoxy. The amount of epoxy used for die attachment is critical and should be sufficient to provide at least 0.002 inches under the chip and to yield a small fillet around its full perimeter. Epoxy dye attachment is performed at room temperature and the device is pressed (lightly) downward without a scrubbing motion.

c. External parts of the part should be inherently non-nutrient to fungus.

d. Internal conductors which are in thermal contact with a substrate along its entire length (such as metallization strips, contact areas, and bonding interfaces) should be designed so that no properly fabricated conductor should experience, at maximum rated current, a current density in excess of the values shown below for the applicable conductor material. This includes allowances for worst case conductor composition, cross-sectional area, normal production tolerances on critical interface dimensions, and actual thickness at critical areas, such as, steps in the elevation or contact windows.

Maximum Allowable Continuous Current Density

| Conductor material | (RMS for pulse applications) |
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| | |
|---|---|
| Aluminum (99.99 percent pure or doped) without glassivation | 2 x 105 amps/cm2 |
| Aluminum (99.99 percent pure or doped) with glassivation | 5 x 105 amps/cm2 |
| Gold | 6 x 105 amps/cm2 |
| All other (unless otherwise specified) | 2 x 105 amps/cm2 |

e. Bonding pads should be metallized and suitable for bonding. From each wafer lot, recommend a sample of at least 5 die, requiring 10 bond wires minimum, be sampled.

f. Internal surfaces should be capable of resisting progressive degradation within a hermetically sealed package. External metal surfaces should be corrosion resistant or shall be plated or treated to resist corrosion. Package material should be free of burrs and other potential particle contamination.

g. External metallic package elements other than leads and terminals (e.g., lids, covers, bases, and seal rings) shall meet applicable environmental requirements without additional finishing of the base materials or be finished to meet those requirements.

h. Standard screw threads listed in FED-STD-H28 should be used for all semiconductors where screw threads are a mechanical requirement.

i. All silicon transistors with "maximum rating" of less than 4 watts at TC of +25°C should have an inorganic transparent protective overlay material on the active metallization (excluding the bonding pads). The glassivation should cover all electrical conductors on the chip except the bonding pads.

j. Parts should be capable of passing the solderability test in accordance with MIL-STD-750 or equivalent method.

k. Die should be stored in dry nitrogen or an inert atmosphere.

l. Thermocompression wedge bonds should not be utilized when aluminum wire is used. For GaAs-based parts, thermocompression wedge bonding with 1.0 mil gold wire is recommended for all packaged FETs, and wire bonding of FETs on test carriers. Ball bonding is not recommended.