MICROELECTRONICS INTEGRITY MEETING AGENDA

Meeting Date & Time: 27 July 2016 @ 0800-1200
Meeting Location: Westin Hotel – Indianapolis, Indiana Rev 17

0730 Coffee

0800 Day 2 Kickoff – Mr. Brian Stuffle, NSWC Crane

0810 Keynote Speaker: Mr. Robert A. Gold, Director, Engineering Enterprise, OUSD (AT&L)/ASD(R&E)/Systems Engineering

0845 Panel 1: **Defense Microelectronics Industrial Base** (Chair – Mr. Roger Smith) - The industrial base continues to migrate offshore, and the pace of technology advancement continue to accelerate. Both of these realities are creating challenges that affect critical DoD system availability, superiority and trustworthiness. Panelists will provide their insights into the state of the industrial base and technology, and will provide their thoughts on the domestic industry's ability to continue to deliver critical and advanced defense technologies.
Speakers & Topics:

- Dr. Robert Irie, Microelectronics Industry Analyst, Manufacturing and Industrial Base Policy Assessments Group, OSD
- Mr. David Bergman, Vice President for Standards and Training, IPC
- Mr. Daniel Marrujo, Lead Microelectronics Reliability Engineer and ORTA, Defense Microelectronics Activity

1000 Break

1030 Panel 2: **Trusted Microelectronics Activities** (Chair - Mr. Brett Hamilton)
This panel will provide an overview of activities geared to help ensure trust in the use of microelectronics manufactured in a global supply chain. The Assistant Secretary of Defense Research and Engineering (ASD(R&E)) engage with Naval Surface Warfare Center (NSWC) Crane (lead execution activity), and DoD laboratories, industry and academia to: 1) Protect critical designs and IP from espionage/manipulation, 2) Advance capability to perform hardware analysis, e.g., physical, functional, and design verification and validation, of critical components for microelectronics trust, 3) Develop commercial standards and practices to design trust in, and 4) Eliminate sole-source dependence on GF Trusted Foundry through development of new trust model that leverages and ensures future access to commercial SOTA microelectronics capabilities.

- Mr. Robert A. Gold, Director, Engineering Enterprise, OUSD(AT&L)/ASD(R&E)/Systems Engineering
- Mr. Matthew Casto, Senior Electronics Engineer, Air Force Research Laboratory, Sensors Directorate, Avionics Vulnerability Mitigation Branch
- Mr. Adam Hauch, Defense Security Service, Counterintelligence Analyst, Defense Security Service

1145 Wrap Up/ Final Comments

1200 Adjourn